NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE2060K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

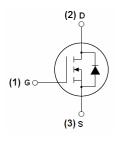
- V_{DS} =20V,I_D =60A
 - $R_{DS(ON)}$ <6m Ω @ V_{GS} =4.5V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE2060K	NCE2060K	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _G s	±12	V
Drain Current-Continuous	I _D	60	А
Drain Current-Continuous(T _C =100°C)	I _D (100℃)	42	Α
Pulsed Drain Current	I _{DM}	210	Α
Maximum Power Dissipation	P _D	60	W
Derating factor		0.48	W/°C
Single pulse avalanche energy (Note 5)	E _{AS}	200	mJ
Operating Junction and Storage Temperature Range	T_{J} , T_{STG}	-55 To 150	$^{\circ}$



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Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	R _{0JC}	2.1	°C/W
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Electrical Characteristics (T_C=25°C unless otherwise noted)

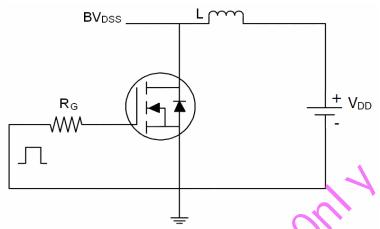
Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250µA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V,V _{GS} =0V	-	-	1	μΑ
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	0.5	0.75	1.0	V
Drain-Source On-State Resistance	В	V _{GS} =4.5V, I _D =20 A	-7	4.8	6	mΩ
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =2.5V, I _D =15A		6.2	9	mΩ
Forward Transconductance	g FS	V _{DS} =10V,I _D =20A	15	-	-	S
Dynamic Characteristics (Note4)		0,				
Input Capacitance	C _{lss}	V _{DS} =10V,V _{GS} =0V,	-	2000	-	PF
Output Capacitance	Coss	$V_{DS} = 10V, V_{GS} = 0V,$ $F = 1.0MHz$	-	500	-	PF
Reverse Transfer Capacitance	C _{rss}	F= F.UVIDZ	-	200	-	PF
Switching Characteristics (Note 4)		0.0				
Turn-on Delay Time	t _{d(on)}		-	6.4	-	nS
Turn-on Rise Time	t	V_{DD} =10 V , I_D =2 A , R_L =1 Ω	-	17.2	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =4.5 V , R_{G} =3 Ω	-	29.6	-	nS
Turn-Off Fall Time	t _f		-	16.8	-	nS
Total Gate Charge	Q_g	\/ -40\/ -20 \	-	27		nC
Gate-Source Charge	Q_{gs}	V_{DS} =10V, I_D =20A, V_{GS} =10V	-	6.5		nC
Gate-Drain Charge	Q_{gd}	V _{GS} -10V	-	6.4		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V _{GS} =0V,I _S =10A	-		1.2	V
Diode Forward Current (Note 2)	Is		-	-	60	Α
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 20A	-	25	-	nS
Reverse Recovery Charge	Qrr	di/dt = 100A/μs ^(Note3)	-	24	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD				

Notes:

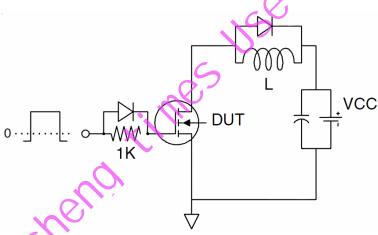
- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- **2.** Surface Mounted on FR4 Board, $t \le 10$ sec.
- **3.** Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2%.
- 4. Guaranteed by design, not subject to production
- **5.** E_{AS} condition : Tj=25 $^{\circ}$ C,V_{DD}=10V,V_G=10V,L=0.5mH,Rg=25 Ω ,

Test circuit

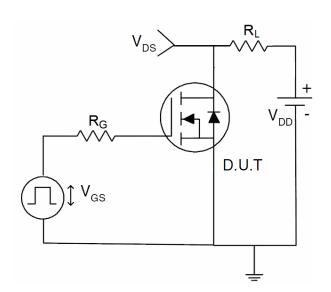
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit





Typical Electrical and Thermal Characteristics (Curves)

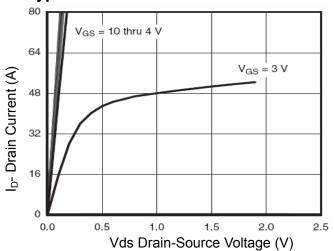


Figure 1 Output Characteristics

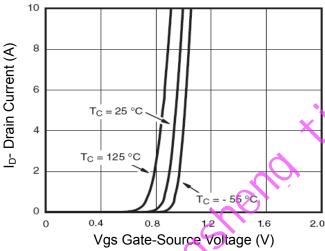


Figure 2 Transfer Characteristics

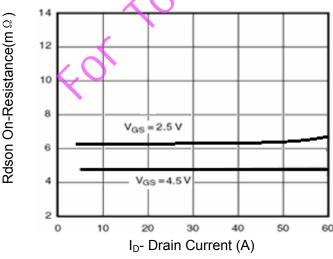


Figure 3 Rdson- Drain Current

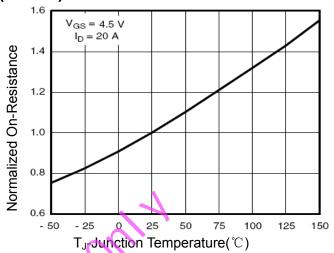


Figure 4 Rdson-JunctionTemperature

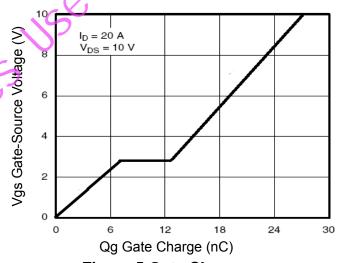


Figure 5 Gate Charge

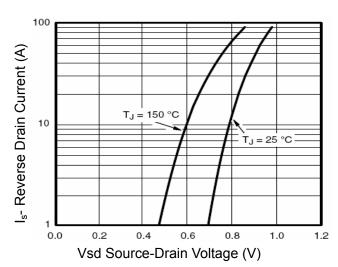
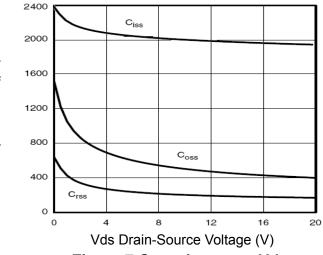


Figure 6 Source- Drain Diode Forward



C Capacitance (pF)



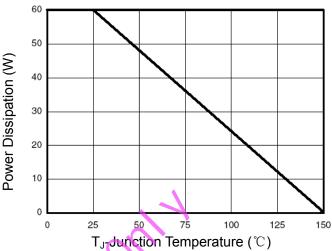
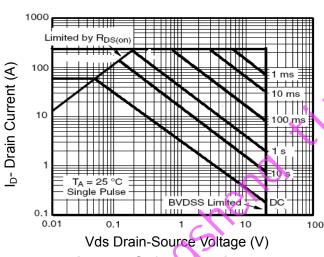


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating



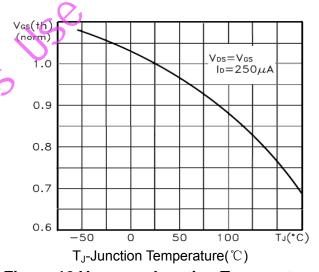


Figure 8 Safe Operation Area

Figure 10 V_{GS(th)} vs Junction Temperature

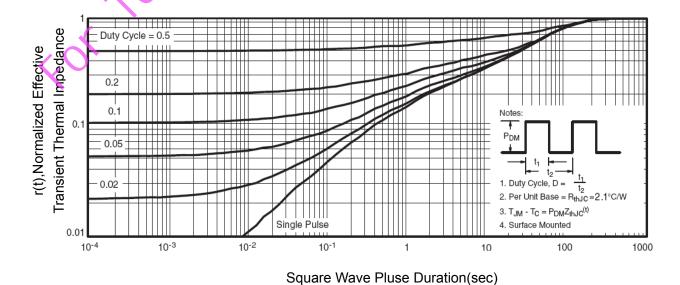
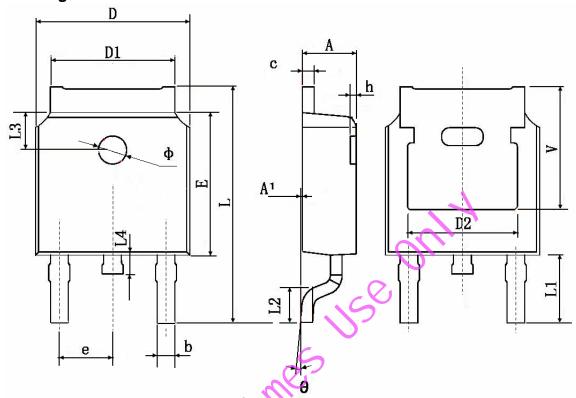


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions I	n Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
A	2.200	2.400	0.087	0.094	
A1	0.000	0.127	0.000	0.005	
b	0.660	0.860	0.026	0.034	
С	0.460	0.580	0.018	0.023	
D	6.500	6.700	0.256	0.264	
D1	5.100	5.460	0.201	0.215	
D2 /	4.830	TYP.	0.190 TYP.		
E	6.000	6.200	0.236	0.244	
e 🇸	2.186	2.386	0.086	0.094	
10,	9.800	10.400	0.386	0.409	
L1	2.900 TYP.		0.114 TYP.		
L2	1.400	1.700	0.055	0.067	
L3	1.600 TYP.		0.063 TYP.		
L4	0.600	1.000	0.024	0.039	
Ф	1.100	1.300	0.043	0.051	
θ	0°	8°	0°	8°	
h	0.000	0.300	0.000	0.012	
V	5.350 TYP.		0.211 TYP.		



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