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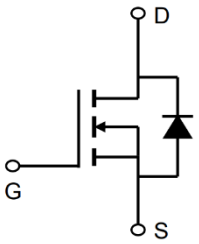
APM
A Power Microelectronics

AP80N03NF

30V N-Channel Enhancement Mode MOSFET

Description

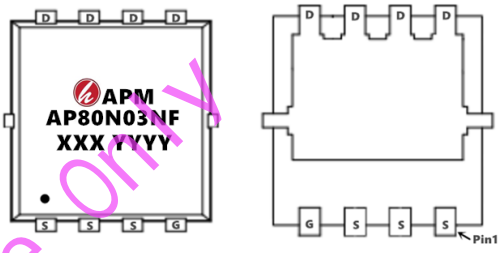
The AP80N03NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

V_{DS} = 30V I_D =80A

$R_{DS(ON)}$ < 4.0mΩ @ V_{GS}=10V

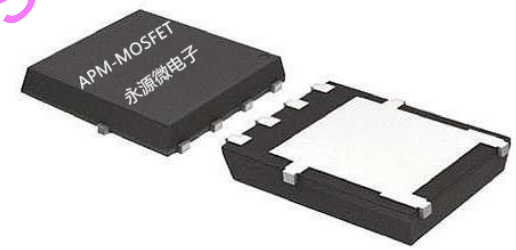


Application

Battery protection

Load switch

Uninterruptible power supply



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Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP80N03NF	PDFN5*6-8L	AP80N03NF XXX YYYY	5000

Absolute Maximum Ratings (TC=25℃unless otherwise noted)

Symbol	Parameter	Max	Units
VDSS	Drain-Source Voltage	30	V
VGSS	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	80	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ 10V[1,6]	65	A
IDM	Pulsed Drain Current note1	400	A
EAS	Single Pulsed Avalanche Energy note2	320	mJ
IAS	Avalanche Current	45.8	A
TSTG	Storage Temperature Range	-55 to 175	℃
T_J	Operating Junction Temperature Range	-55 to 175	℃
P_D@T_C=25℃	Total Power Dissipation[4]	88	W
P_D@T_A=25℃	Total Power Dissipation[4]	44	W
RθJA	Thermal Resistance Junction-Ambient [1]	58	℃/W
RθJA	Thermal Resistance Junction-Ambient [1] (t ≤10s)	20	℃/W
RθJC	Thermal Resistance Junction-Case[1]	2.3	℃/W

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Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	30	-	-	V
IDSS	Zero Gate Voltage Drain Current	V_{DS} =30V, V_{GS} = 0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V_{DS} =0V,V_{GS} = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.5	V
RDS(on)	Static Drain-Source on-Resistance	V_{GS} =10V, I_D =24A	-	2.9	4.0	mΩ
RDS(on)	Static Drain-Source on-Resistance	V_{GS} =4.5V, I_D =12A	-	5.3	6.5	
RG	Gate resistance	V_{GS}=0V,V_{DS}=0V,f=1.0MHz			3.3	Ω
gFS	Forward Transconductance	V_{DS} =10V, I_D =10A	-	15.5	-	S
Ciss	Input Capacitance	V_{DS} =25V, V_{GS} =0V, f = 1.0MHz	-	2200	-	pF
Coss	Output Capacitance		-	280	-	pF
Crss	Reverse Transfer Capacitance		-	177	-	pF
Q_g	Total Gate Charge	V_{DS} =15V, I_D =24A, V_{GS} =10V	-	42	-	nC
Qgs	Gate-Source Charge		-	4	-	nC
Qgd	Gate-Drain(“Miller”) Charge		-	13	-	nC
td(on)	Turn-on Delay Time	V_{DD}=15V, I_D=15A, R_{GEN}=3.3Ω, V_{GS} =10V	-	12.6	-	ns
t_r	Turn-on Rise Time		-	19.5	-	ns
td(off)	Turn-off Delay Time		-	42.8	-	ns
t_f	Turn-off Fall Time		-	13.2	-	ns
IS	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	-	-	100	A
ISM	Pulsed Source Current[2,5]		-	-	400	A
VSD	Diode Forward Voltage[2]	V_{GS} = 0V, I_S=30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I_F=30A,dI/dt=100A/μs	-	19	-	ns
Qrr	Body Diode Reverse RecoveryCharge		-	11	-	nC

Note :
1.The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The EAS data shows Max. rating . The test condition is VDD =25V,V GS =10V,L=0.1mH,I AS =45.8A
4.The power dissipation is limited by 175℃ junction temperature
5.The data is theoretically the same as I D and I DM , in real applications , should be limited by total power dissipation.
6.Package limitation current is 85A.

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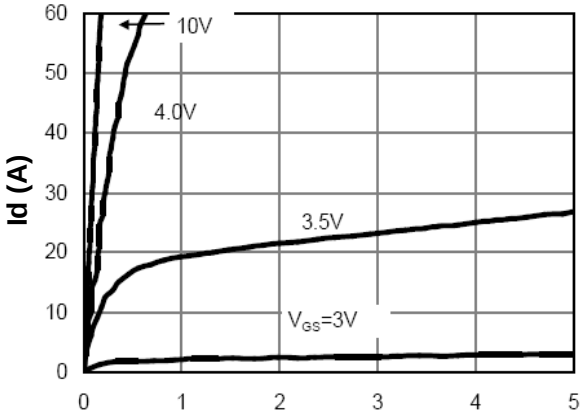
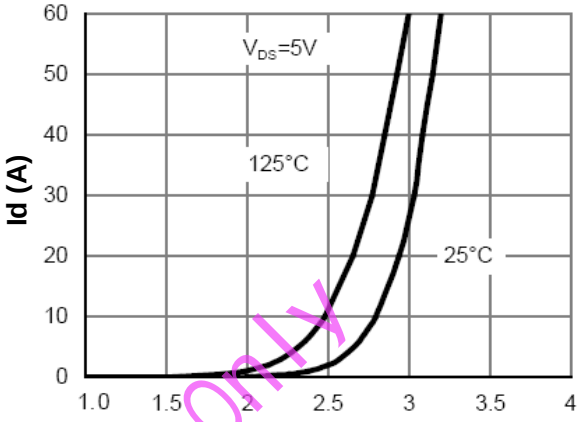
Typical Characteristics



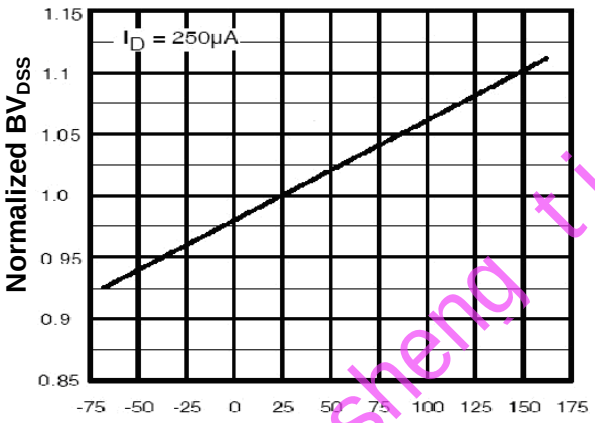
VDS Drain-to-Source Voltage(V)

Figure 1. Output Characteristics



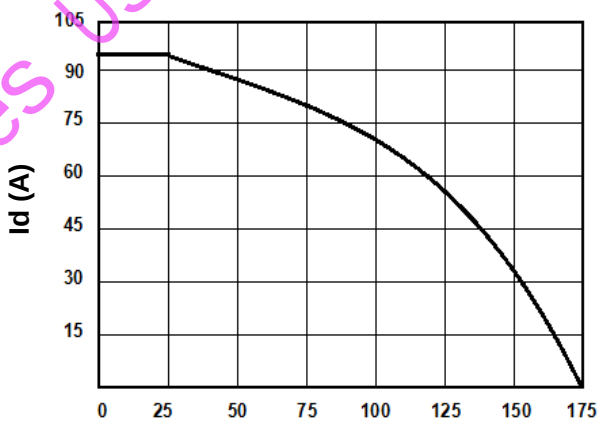
VGS Gate-to-Source Voltage(V)

Figure 2. Transfer Characteristics



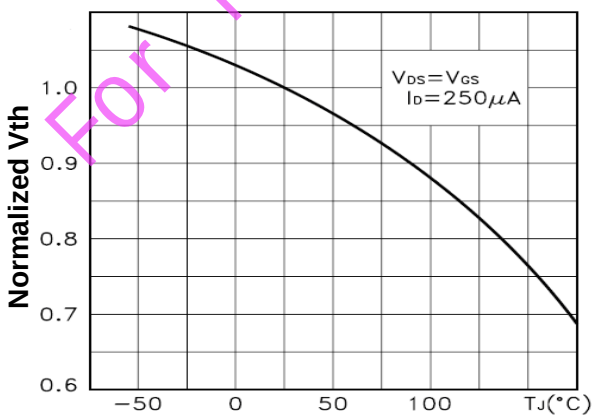
T_J-Junction Temperature(℃)

Figure 3. Max BV_{DSS} vs Junction Temperature



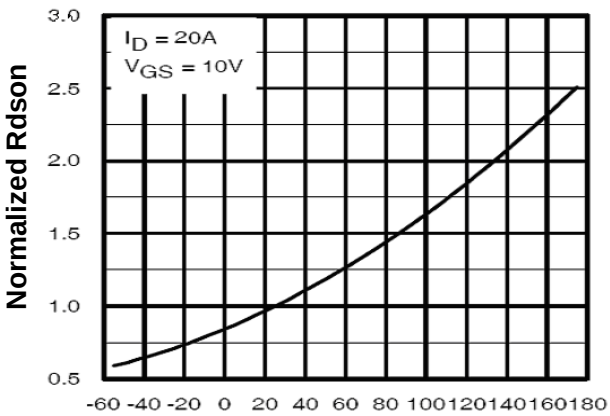
T_J-Junction Temperature(℃)

Figure 4. Drain Current



T_J-Junction Temperature(℃)

Figure 5. $V_{GS(th)}$ vs Junction Temperature



T_J-Junction Temperature(℃)

Figure 6. $R_{DS(ON)}$ vs Junction Temperature

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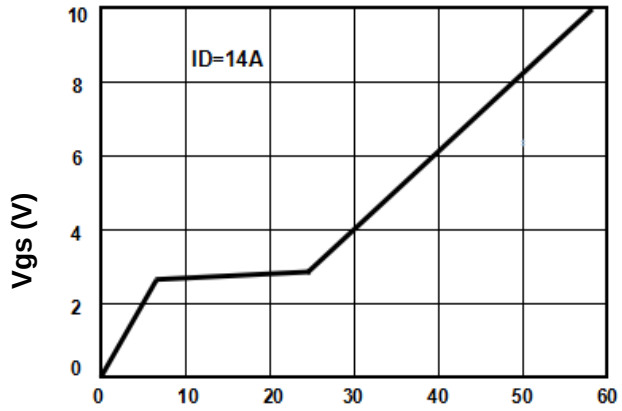

Figure 7. Gate Charge Waveforms

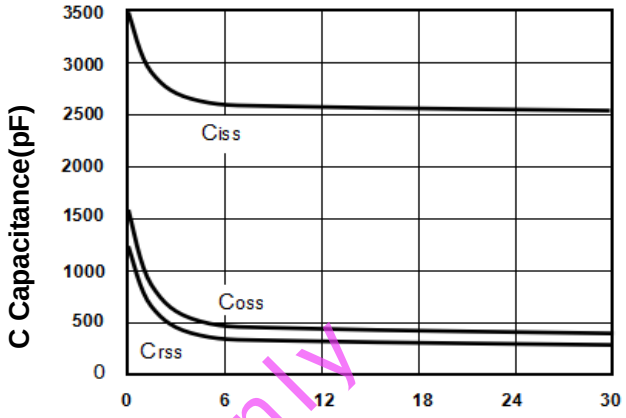

Figure 8. Capacitance

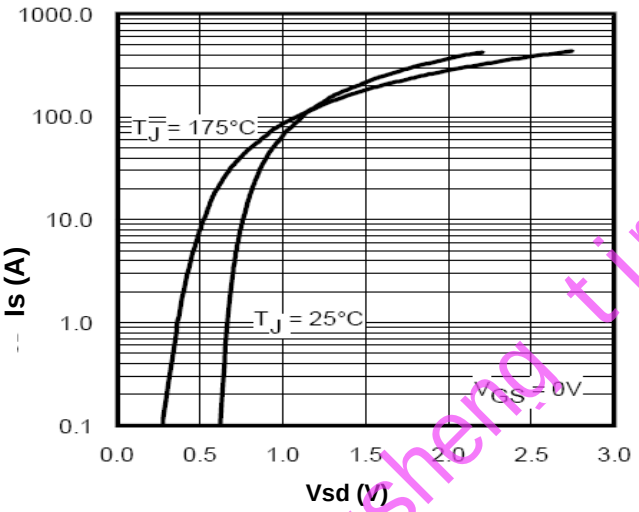

Figure 9. Body-Diode Characteristics

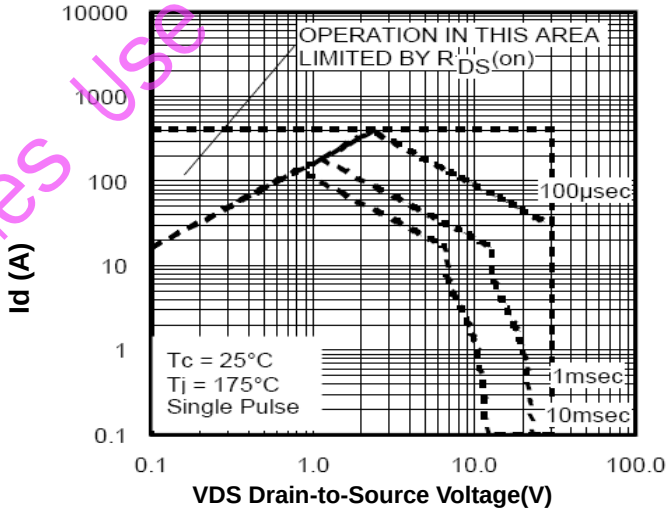

Figure 10. Maximum Safe Operating Area

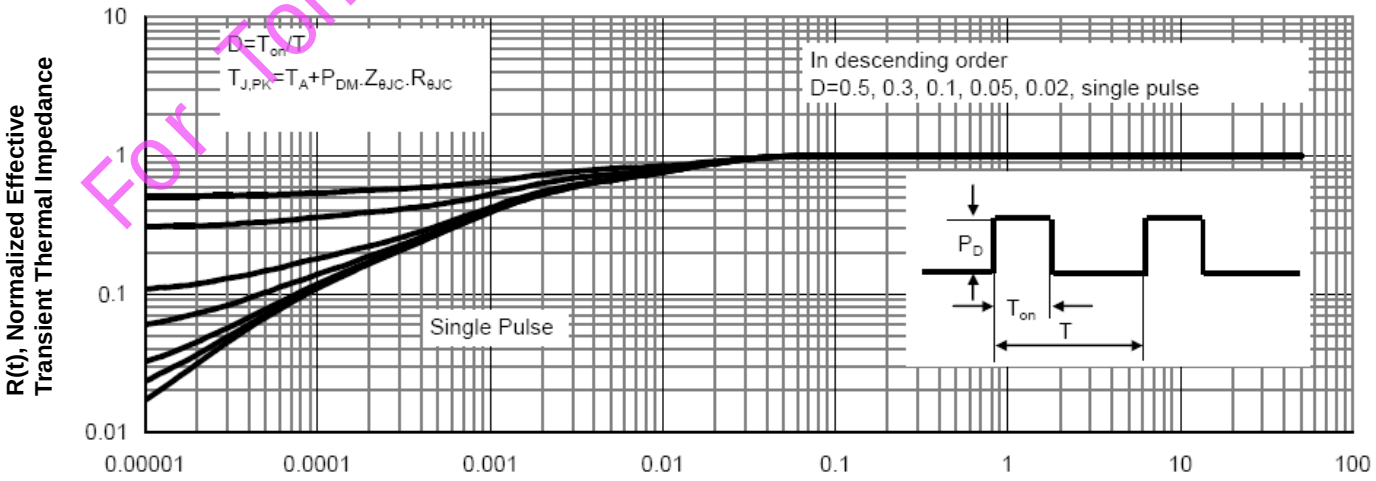

Figure 11. Normalized Maximum Transient Thermal Impedance

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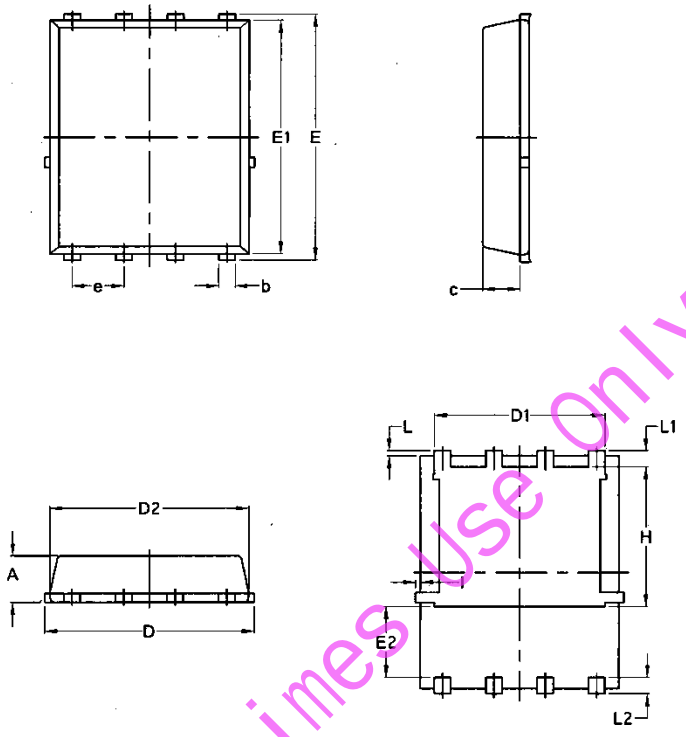
Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070

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30V N-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2019/8/1	Initial release

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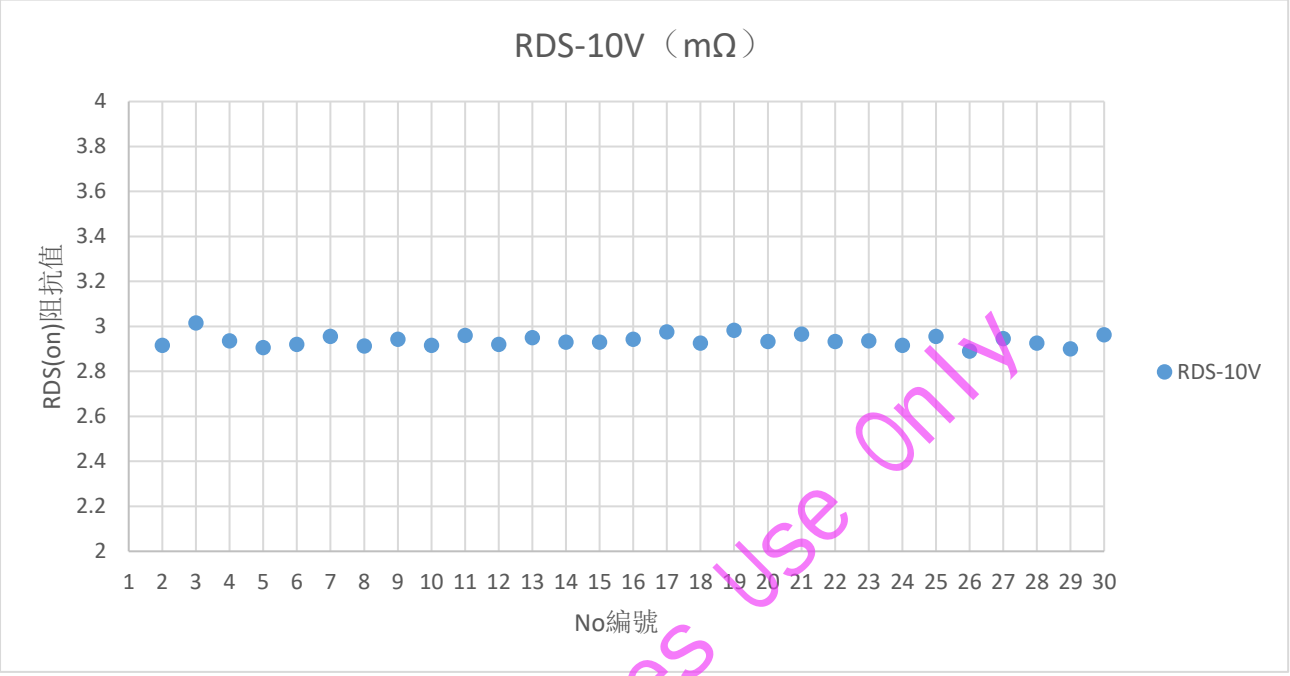
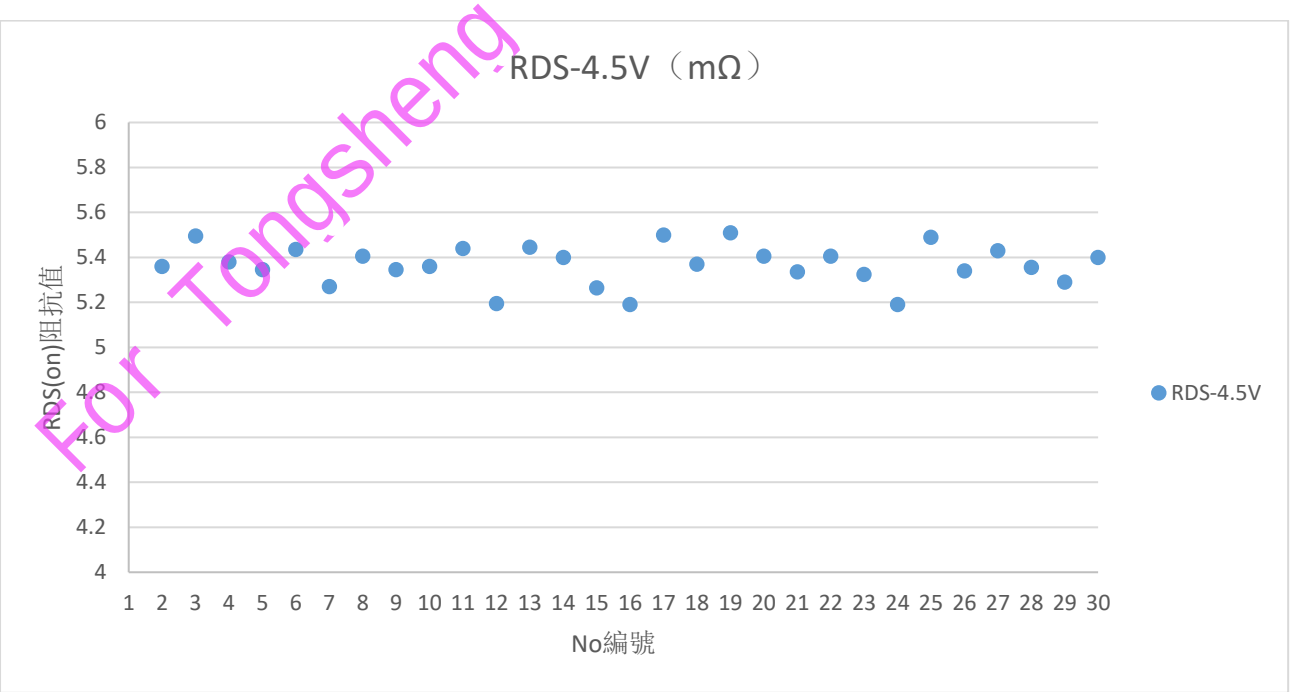
Test Report For 30PCS（30pcs 典型測試報告）





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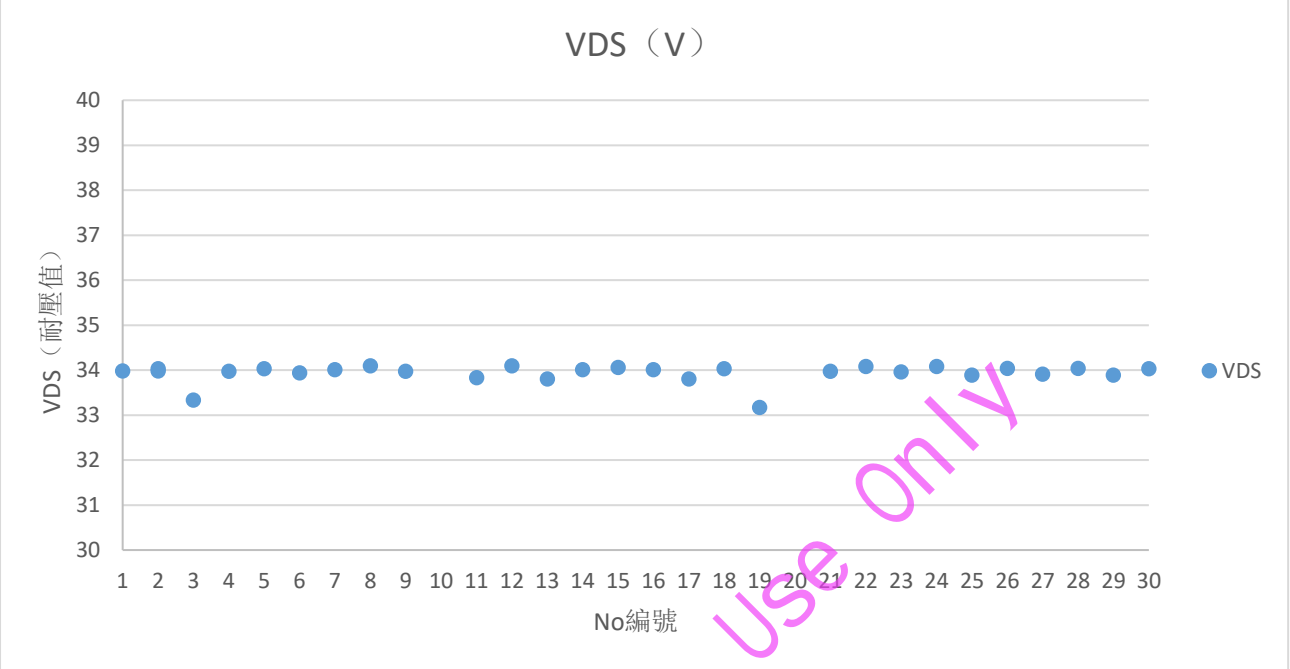

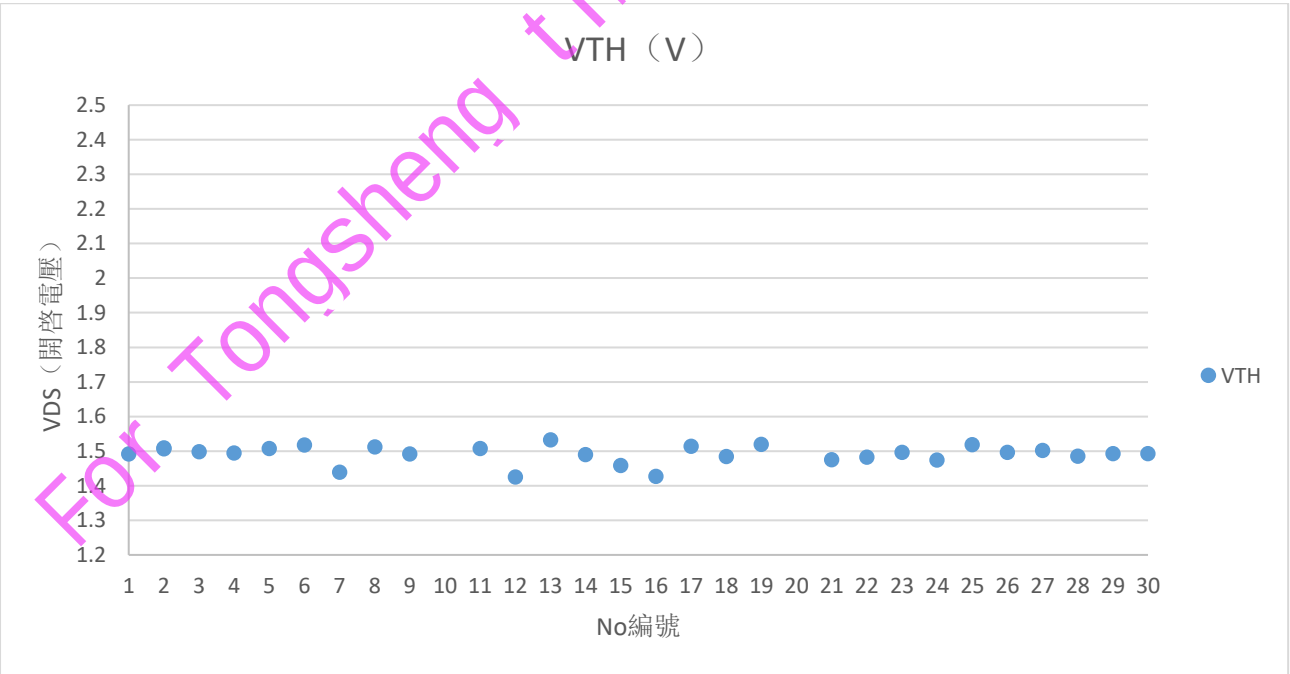

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