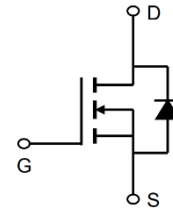


## 40V N-Channel Enhancement Mode MOSFET

### Description

The AP80N04D uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



### General Features

$V_{DS} = 40V$   $I_D = 80A$

$R_{DS(ON)} < 7.5m\Omega @ V_{GS}=10V$

### Application

Battery protection

Load switch

Uninterruptible power supply

### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP80N04D	TO-252-3L	AP80N04D XXX YYYY	2500

### Absolute Maximum Ratings (T<sub>c</sub>=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	40	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D@T<sub>c</sub>=25°C</sub>	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	80	A
I <sub>D@T<sub>c</sub>=100°C</sub>	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>1</sup>	45	A
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	120	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>3</sup>	76.1	mJ
I <sub>AS</sub>	Avalanche Current	39	A
P <sub>D@T<sub>c</sub>=25°C</sub>	Total Power Dissipation <sup>4</sup>	44.6	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C
R <sub>θJA</sub>	Thermal Resistance Junction-ambient (Steady State) <sup>1</sup>	62	°C/W
R <sub>θJC</sub>	Thermal Resistance Junction-Case <sup>1</sup>	2.8	°C/W



**40V N-Channel Enhancement Mode MOSFET****Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

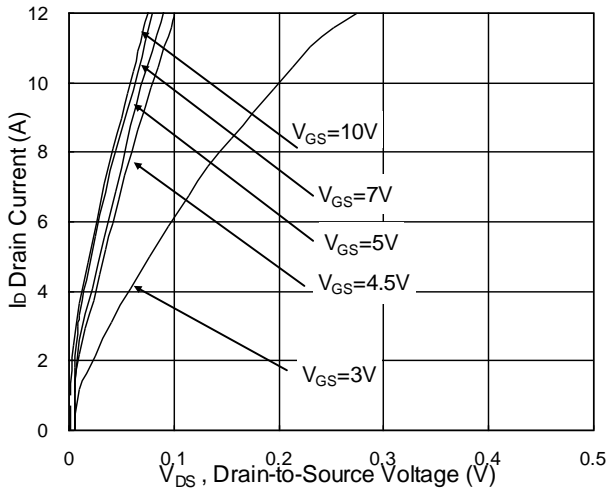
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	40	47	---	V
ΔBVDSS/ΔT <sub>J</sub>	BVDSS Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	---	0.034	---	V/°C
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =12A	---	6.0	7.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	---	9.0	12	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	1.5	2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	-4.96	---	mV/°C
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
IGSS	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =12A	---	39	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	1.6	---	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =20V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =12A	---	18.8	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	4.7	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	8.2	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =1A	---	14.3	---	ns
T <sub>r</sub>	Rise Time		---	2.6	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	77	---	
T <sub>f</sub>	Fall Time		---	4.8	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	2332	---	pF
C <sub>oss</sub>	Output Capacitance		---	193	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	138	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	60	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>		---	---	120	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1	V

**Note :**

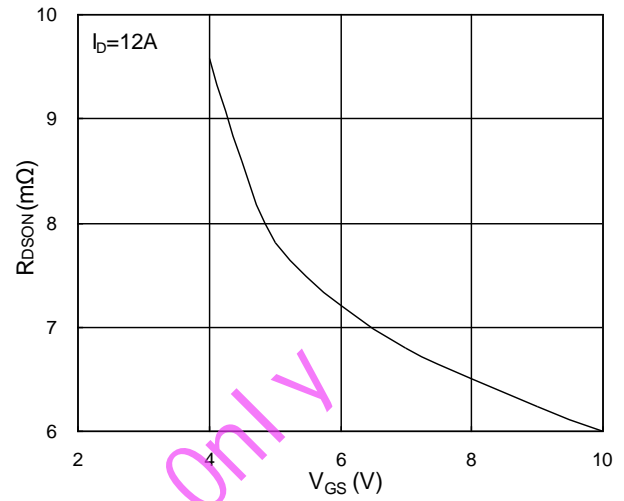
1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%
3. The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=39A
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

## 40V N-Channel Enhancement Mode MOSFET

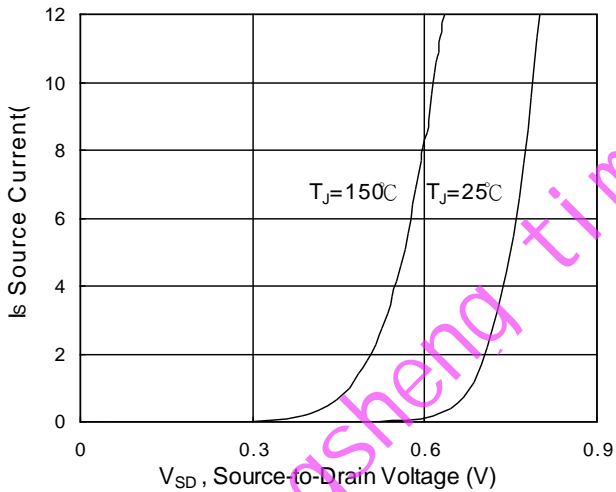
### Typical Characteristics



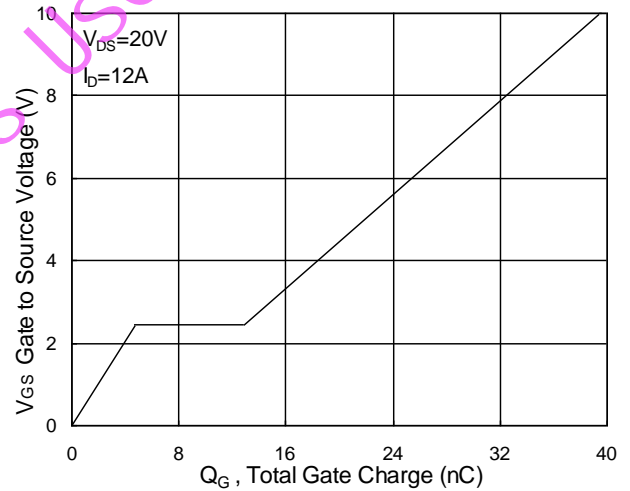
**Fig.1 Typical Output Characteristics**



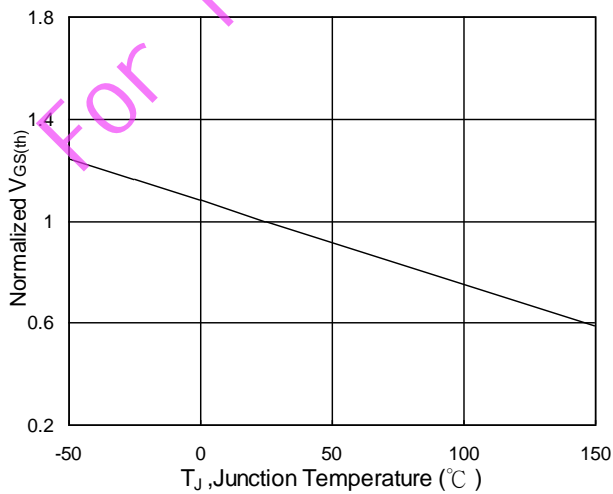
**Fig.2 On-Resistance vs. G-S Voltage**



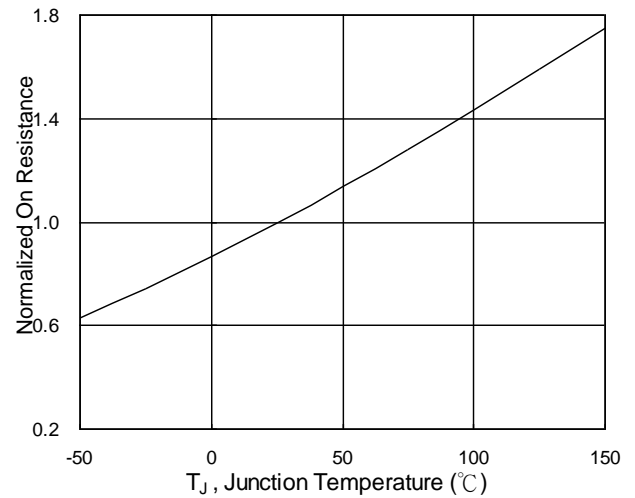
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**



**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

## 40V N-Channel Enhancement Mode MOSFET

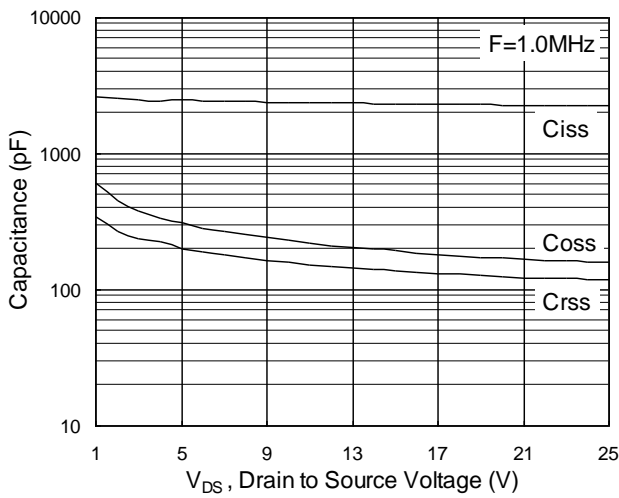


Fig.7 Capacitance

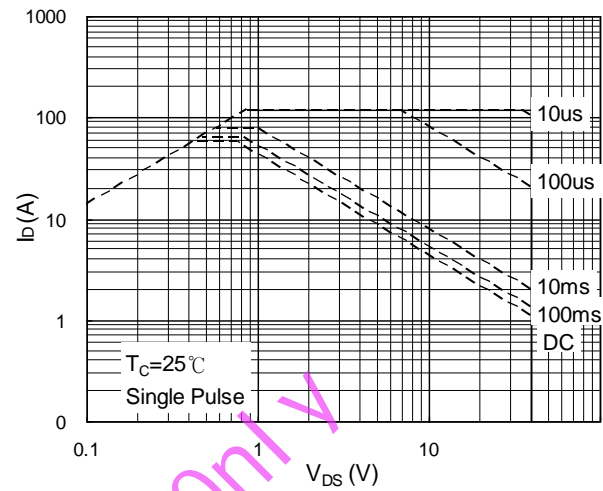


Fig.8 Safe Operating Area

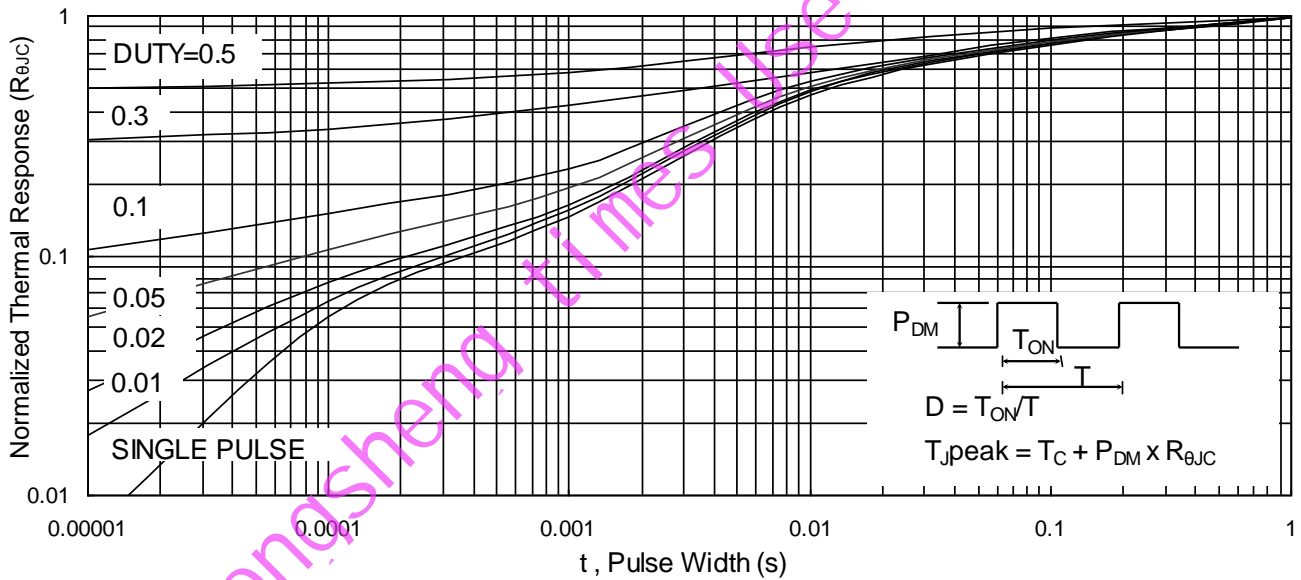


Fig.9 Normalized Maximum Transient Thermal Impedance

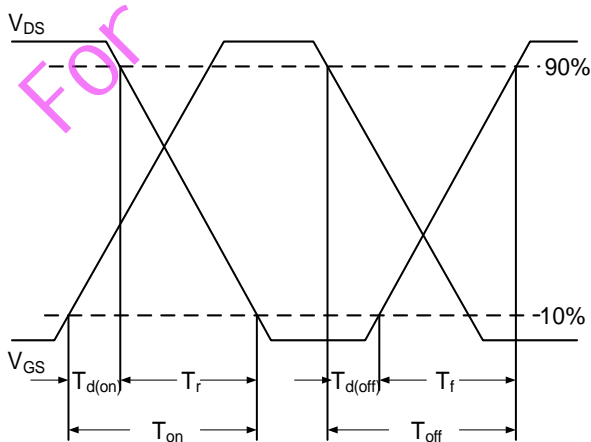


Fig.10 Switching Time Waveform

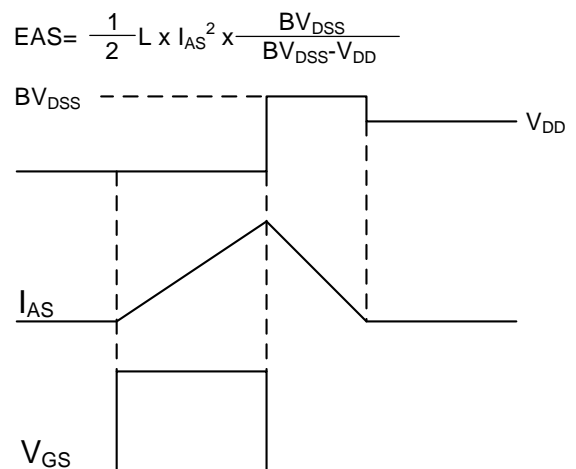
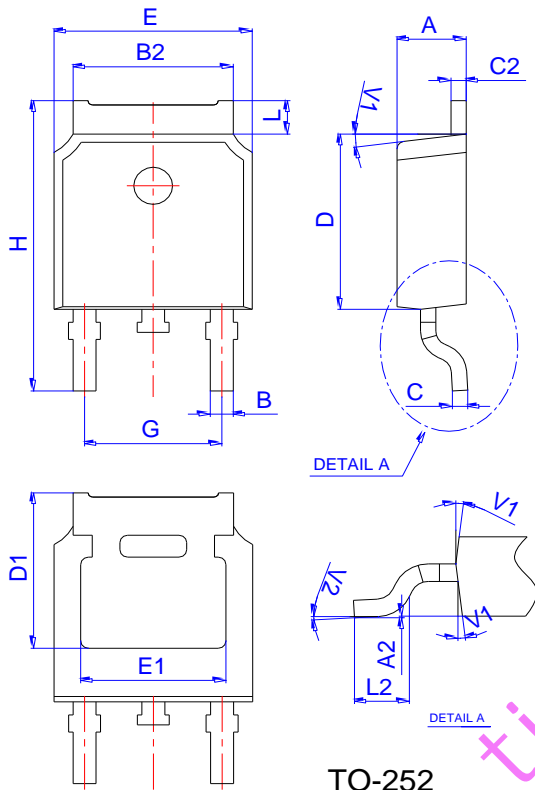


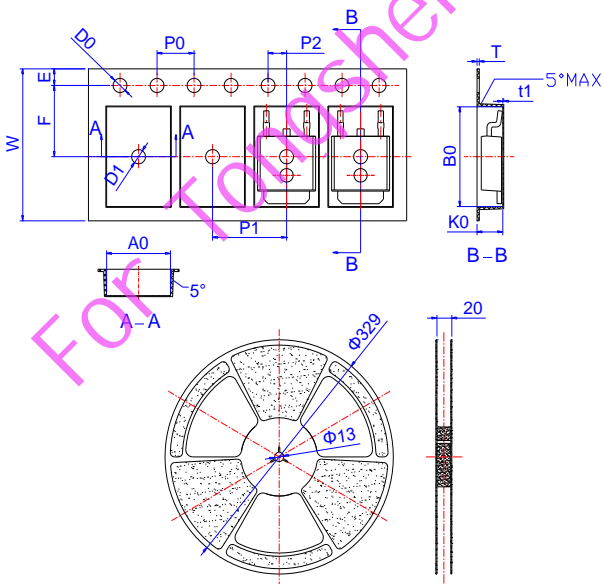
Fig.11 Unclamped Inductive Waveform

### Package Mechanical Data: TO-252-3L



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

### Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

## 40V N-Channel Enhancement Mode MOSFET

### Attention

- 1, Any and all APM Microelectronics products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your APM Microelectronics representative nearest you before using any APM Microelectronics products described or contained herein in such applications.
- 2, APM Microelectronics assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all APM Microelectronics products described or contained herein.
- 3, Specifications of any and all APM Microelectronics products described or contained here instipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- 4, APM Microelectronics Semiconductor CO., LTD. strives to supply high quality high reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- 5, In the event that any or all APM Microelectronics products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- 6, No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of APM Microelectronics Semiconductor CO., LTD.
- 7, Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. APM Microelectronics believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.
- 8, Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the APM Microelectronics product that you intend to use.

## 40V N-Channel Enhancement Mode MOSFET

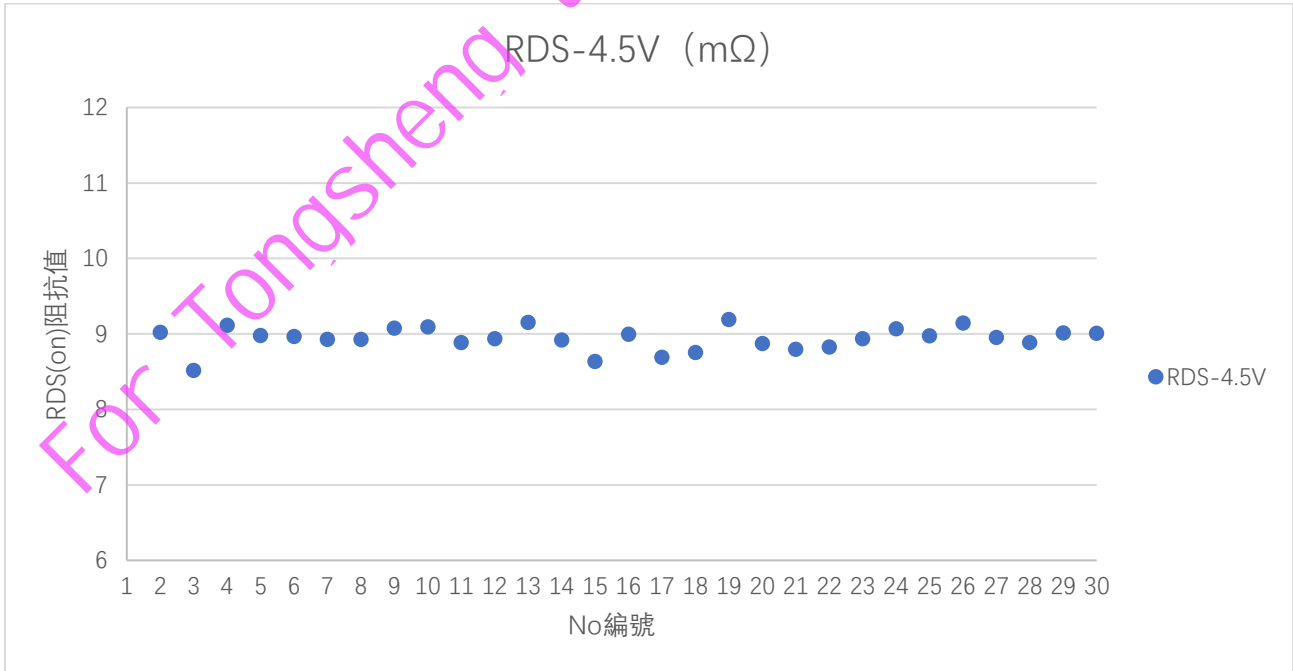
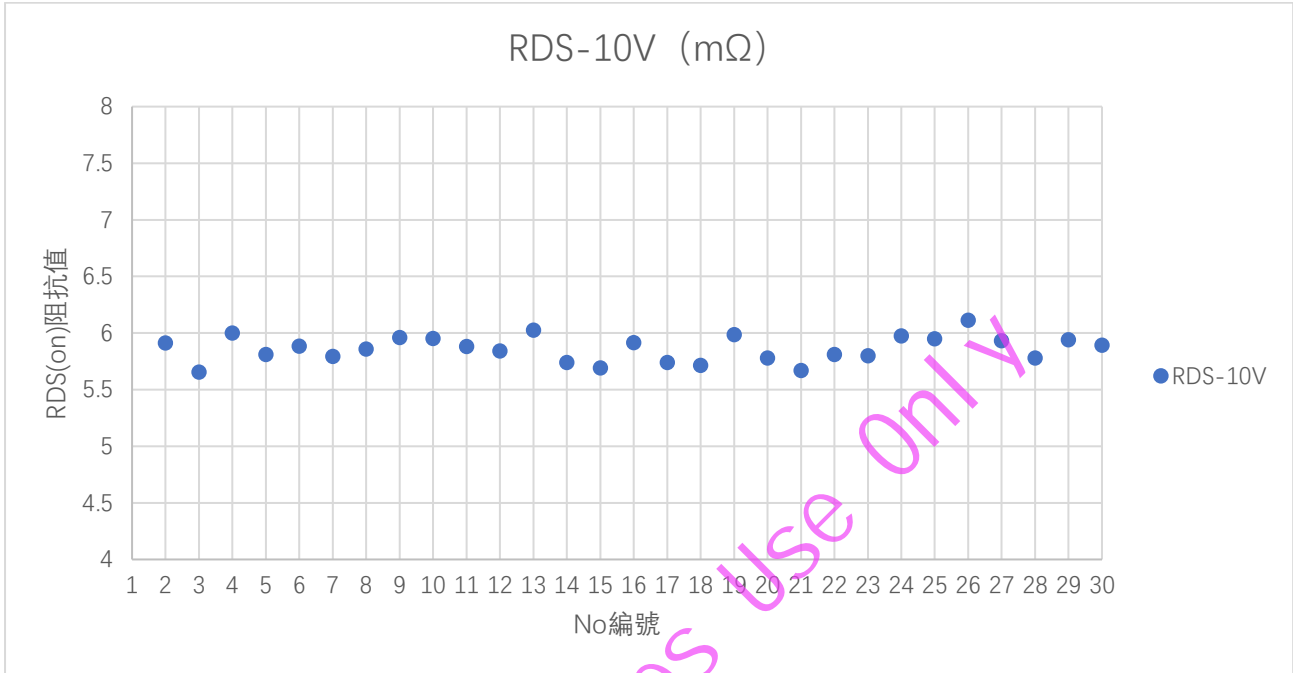
Edition	Date	Change
Rve3.8	2018/1/31	Initial release
Rve3.9	2019/12/01	Reduce RDS(on)

Copyright Attribution "APM-Microelectronic"

For Tongsheng times Use Only



### Test Report For 30PCS (30pcs 典型測試報告)





## 40V N-Channel Enhancement Mode MOSFET

