

### -40V P-Channel Enhancement Mode MOSFET

#### **Description**

The AP5P04MI uses advanced trench technology to provide excellent R<sub>DS(ON)</sub>, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

#### **General Features**

 $V_{DS} = -40V I_{D} = -5.0A$ 

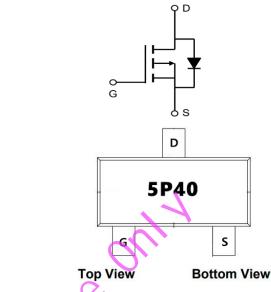
 $R_{DS(ON)} < 72m\Omega$  @  $V_{GS}$ =-10V (Type: 65m $\Omega$ )

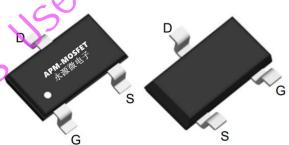
#### **Application**

Battery protection

Load switch

Uninterruptible power supply





Package Marking and Ordering Information

Tuokage marking and Ordering internation				
Product ID	Pack	Marking	Qty(PCS)	
AP5P04MI	SOT23-3L	5P40	3000	

Absolute Maximum Ratings (T<sub>c</sub>=25°Cunless otherwise noted)

Symbol	Parameter	Steady State	Units
VDS /	Drain-Source Voltage -40		V
VGS	Gate-Source Voltage ±20		V
I <sub>D</sub> @T <sub>A</sub> =25℃	Continuous Drain Current, V <sub>GS</sub> @ -4.5V <sup>1</sup> -5.0		А
I <sub>D</sub> @T <sub>A</sub> =70°C	Continuous Drain Current, V <sub>GS</sub> @ -4.5V <sup>1</sup>	-3.0	А
IDM	IDM Pulsed Drain Current <sup>2</sup> -16.1		А
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>3</sup> 1.32		W
P <sub>D</sub> @T <sub>A</sub> =70°C	Total Power Dissipation <sup>3</sup> 0.84		W
TSTG	TSTG Storage Temperature Range -55 to 150		°C
TJ	T <sub>J</sub> Operating Junction Temperature Range -55 to 150		°C
R <sub>θ</sub> JA	Thermal Resistance Junction-Ambient <sup>1</sup> 125		°C/W
ReJC	R <sub>θ</sub> JC Thermal Resistance Junction-Case <sup>1</sup> 80		°C/W



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#### Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур	Max.	Unit	
BVDSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =-250uA	-40	-46		V	
∆BVDSS/∆TJ	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =-1mA		-0.018		V/°C	
DDG(011)	Static Ducin Service On Besistance <sup>2</sup>	V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-3A		65	72	0	
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-2.5V , I <sub>D</sub> =-2A		89	100	mΩ	
VGS(th)	Gate Threshold Voltage	\/ \/ L 050 A	-1.0	-1.5	-2.5	V	
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA		2.5		mV/°C	
IDSS	Drain-Source Leakage Current	V <sub>DS</sub> =-24V , V <sub>GS</sub> =0V ,T <sub>J</sub> =25°C			-1	uA	
1500	Dialii-Source Leakage Current	V <sub>DS</sub> =-24V , V <sub>GS</sub> =0V ,T <sub>J</sub> =55°C	\		-5	uA	
IGSS	Gate-Source Leakage Current	$V_{GS}$ =±20V , $V_{DS}$ =0V			±100	nA	
gfs	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-3A	2	5.8		S	
Qg	Total Gate Charge (-4.5V)			6.4		nC	
Qgs	Gate-Source Charge	V <sub>DS</sub> =-32V , V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-		2.1			
Qgd	Gate-Drain Charge	0,70		2.5			
Td(on)	Turn-On Delay Time			4.2			
Tr	Rise Time	$V_{DD}$ =-20 $V$ , $V_{GS}$ =-4.5 $V$ ,		23		ns	
Td(off)	Turn-Off Delay Time	Re=3.3Ω, I <sub>D</sub> =-3A		26.8			
T <sub>f</sub>	Fall Time			20.6			
Ciss	Input Capacitance			620			
Coss	Output Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz		65		pF	
Crss	Reverse Transfer Capacitance			53			
IS	Continuous Source Current <sup>1,4</sup>	\/-=\/-=0\/			-5.2	Α	
ISM	Pulsed Source Current <sup>2,4</sup>	· V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	-		-16.1	Α	
VSD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25°C			-1	V	

#### Note:

- 1. The data tested by surface mounted on a 1 inch FR-4 board with 2OZ copper.
- 2. The data tested by pulsed , pulse width  $\leq 300 us$  , duty cycle  $\leq 2\%$
- 3. The power dissipation is limited by 150°C junction temperature
- $4\sqrt{100}$  The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



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## **Typical Characteristics**

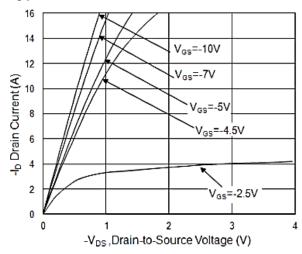


Fig.1 Typical Output Characteristics

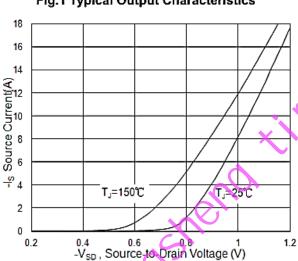


Fig.3 Forward Characteristics Of Reverse

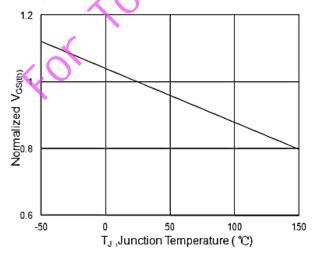


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

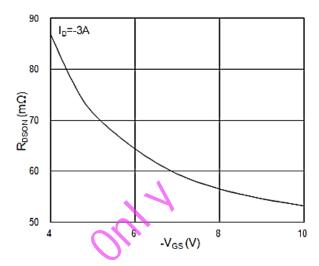


Fig.2 On-Resistance vs. G-S Voltage

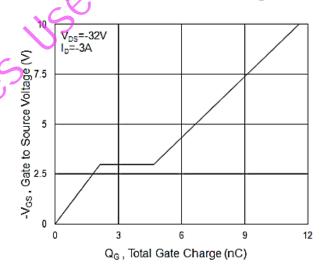


Fig.4 Gate-Charge Characteristics

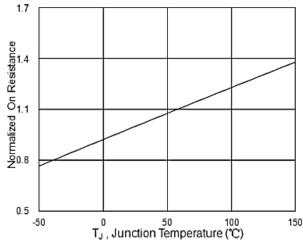
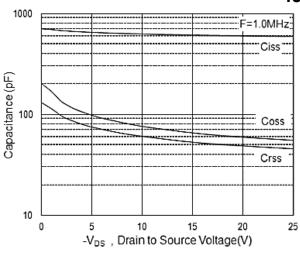


Fig.6 Normalized RDSON vs. TJ





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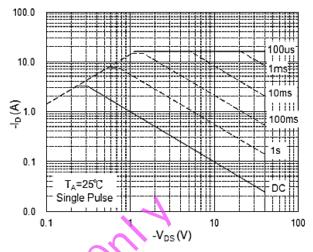


Fig.7 Capacitance

Fig.8 Safe Operating Area

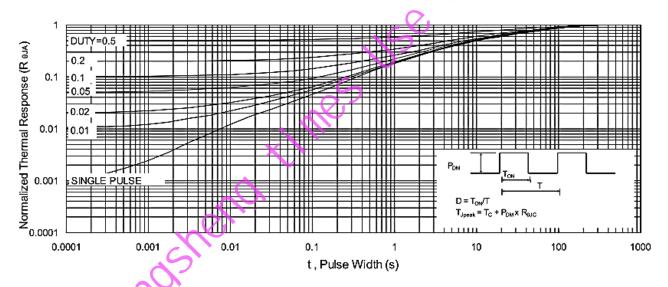
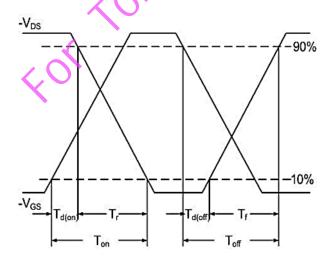


Fig.9 Normalized Maximum Transient Thermal Impedance



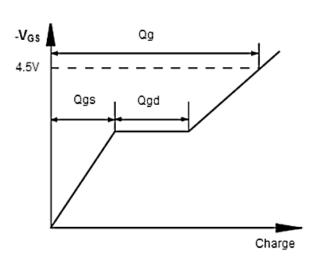


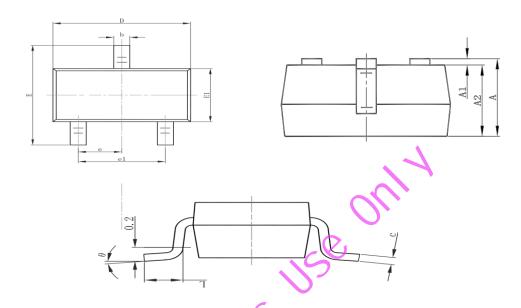
Fig.10 Switching Time Waveform

Fig.11 Gate Charge Waveform



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# Package Mechanical Data:SOT23-3L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
Α	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
С	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
Е	2.650	2.950	0.104	0.116
е	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L /	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°



# -40V P-Channel Enhancement Mode MOSFET Attention

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