APM
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AP50P03NF

30V P-Channel Enhancement Mode MOSFET

Description

The AP50P03NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

V_{DS} = -30V I_D =-50A

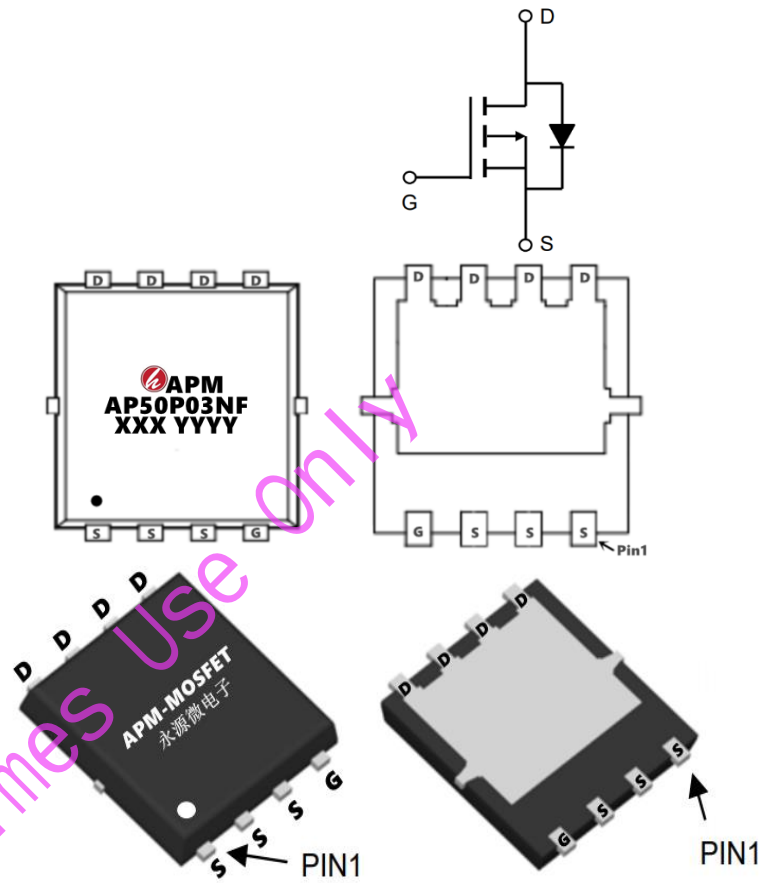
$R_{DS(ON)}$ <13mΩ @ V_{GS}=-10V （**Type：8.8mΩ**）

Application

Lithium battery protection

Wireless impact

Mobile phone fast charging



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP50P03NF	PDFN3*3-8L	AP50P03NF XXX YYYY	5000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	±25	V
I_D@T_C=25℃	Continuous Drain Current, V_{GS} @ -10V[1]	-50	A
I_D@T_C=100℃	Continuous Drain Current, V_{GS} @ -10V[1]	-30	A
I_{DM}	Pulsed Drain Current[2]	-150	A
EAS	Single Pulse Avalanche Energy[3]	125	mJ
I_{AS}	Avalanche Current	-50	A
P_D@T_C=25℃	Total Power Dissipation[4]	45	W
P_D@T_A=25℃	Total Power Dissipation[4]	2.0	W
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	25	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	2.8	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	-33	---	V
△BVDSS/△TJ	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.0232	---	V/℃
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-30A	---	8.8	13	mΩ
		V_{GS}=-4.5V , I_D=-15A	---	14	20	
VGS(th)	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.0	-1.7	-2.5	V
△$V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.6	---	mV/℃
IDSS	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=55℃	---	---	-5	
IGSS	Gate-Source Leakage Current	V_{GS}=±25V , V_{DS}=0V	---	---	±100	nA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-30A	---	30	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	9	---	Ω
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15V , V_{GS}=-4.5V , I_D=-15A	---	22	---	nC
Qgs	Gate-Source Charge		---	8.7	---	
Qgd	Gate-Drain Charge		---	7.2	---	
Td(on)	Turn-On Delay Time	V_{DD}=-15V , V_{GS}=-10V , R_G=3.3Ω I_D=-15A	---	8	---	ns
T_r	Rise Time		---	73.7	---	
Td(off)	Turn-Off Delay Time		---	61.8	---	
T_f	Fall Time		---	24.4	---	
Ciss	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	2215	---	pF
Coss	Output Capacitance		---	310	---	
Crss	Reverse Transfer Capacitance		---	237	---	
IS	Continuous Source Current[1,5]	V_G=V_D=0V , Force Current	---	---	-45	A
ISM	Pulsed Source Current[2,5]		---	---	-150	A
VSD	Diode Forward Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	---	-1	V
trr	Reverse Recovery Time	IF=-15A , dI/dt=100A/μs , T_J=25℃	---	19	---	nS
Q_{rr}	Reverse Recovery Charge		---	9	---	nC

Note :

1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 2OZ copper.

2、The data tested by pulsed , pulse width .The EAS data shows Max. rating .

3、The power dissipation is limited by 175℃ junction temperature

4、EAS condition: TJ=25℃, VDD= -24V, VG= -10V, RG=7Ω, L=0.1mH, IAS= -50A

5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics

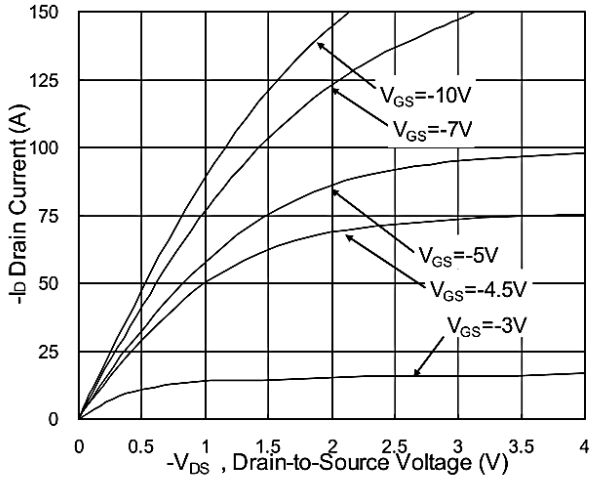


Fig.1 Typical Output Characteristics

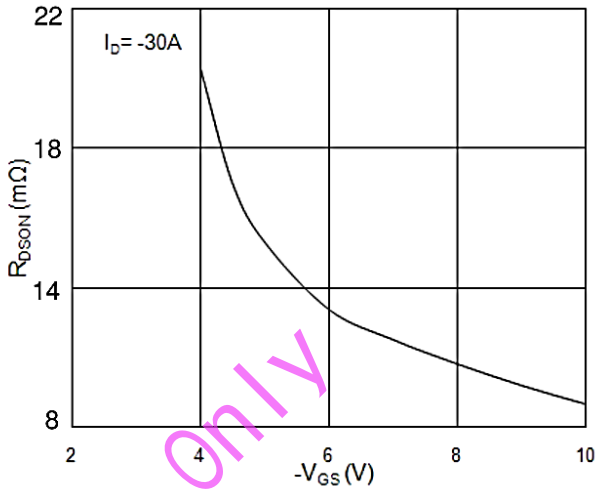


Fig.2 On-Resistance vs. G-S Voltage

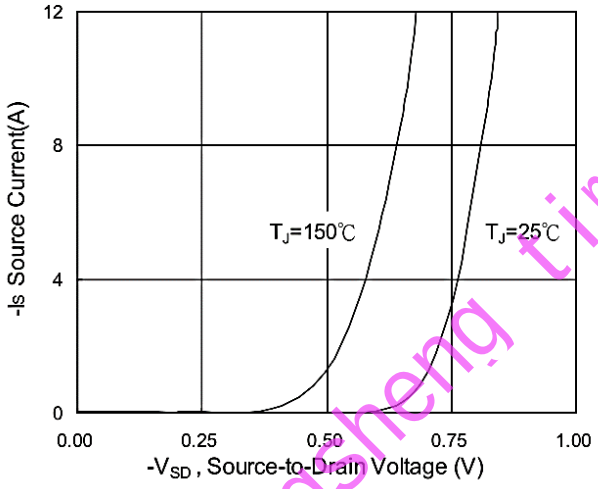


Fig.3 Forward Characteristics of Reverse

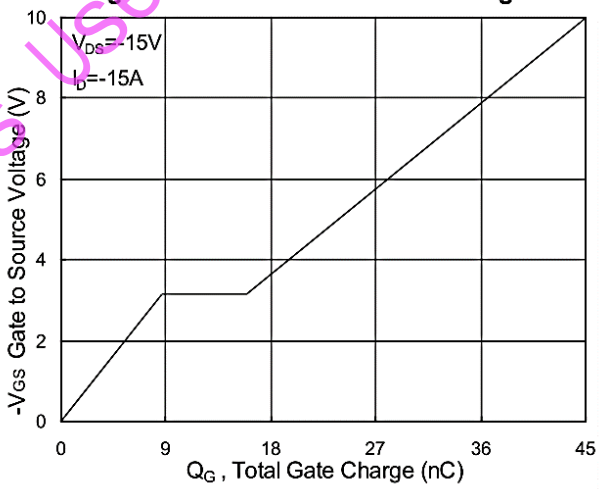


Fig.4 Gate-Charge Characteristics

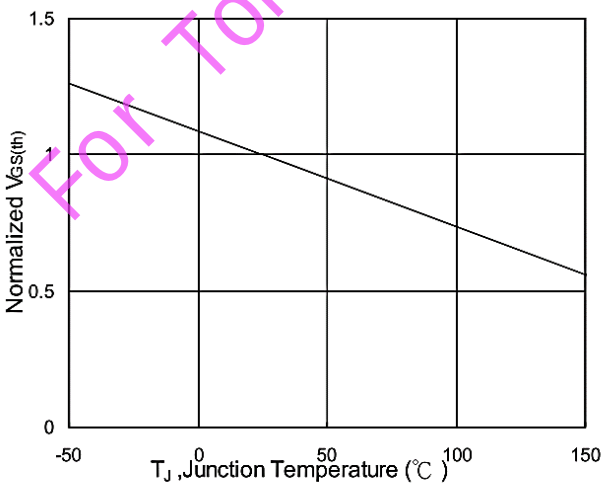


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

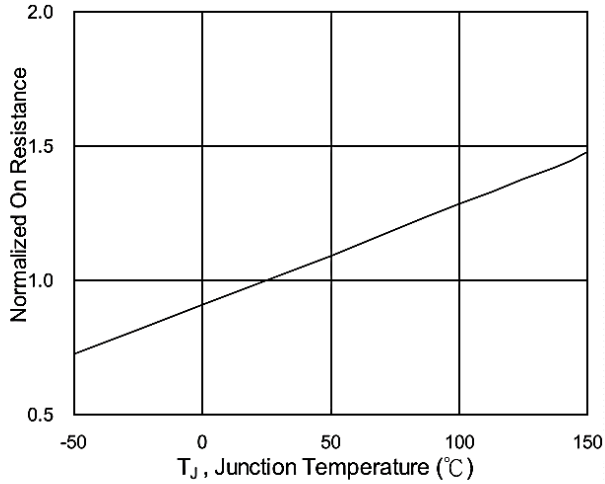


Fig.6 Normalized R_{DSON} vs. T_J

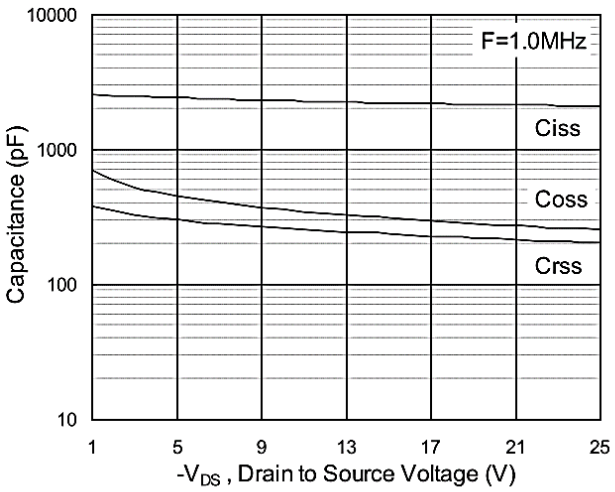


Fig.7 Capacitance

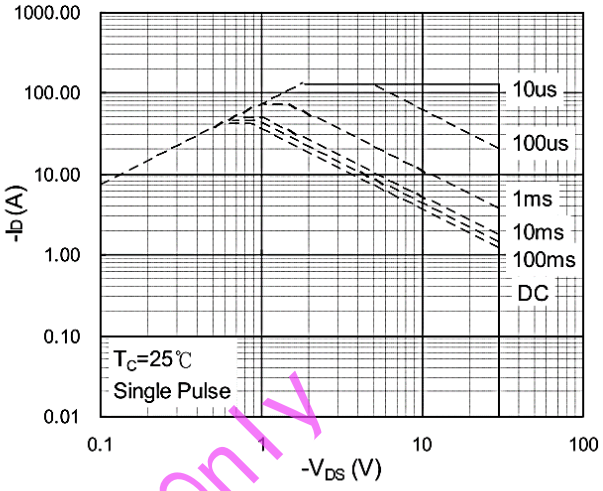


Fig.8 Safe Operating Area

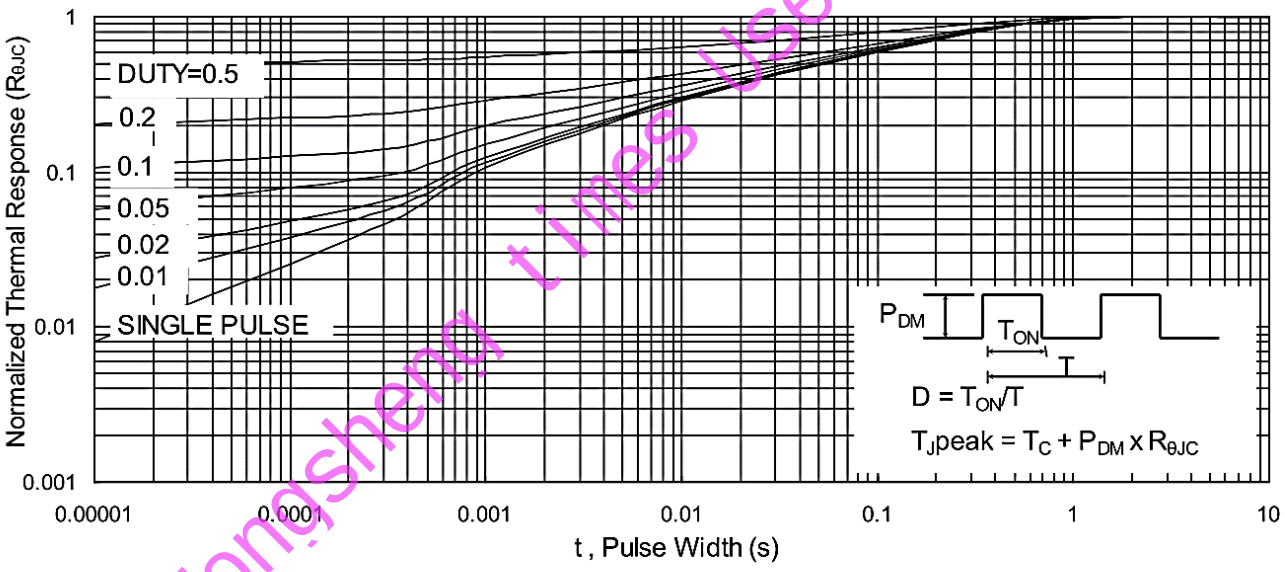


Fig.9 Normalized Maximum Transient Thermal Impedance

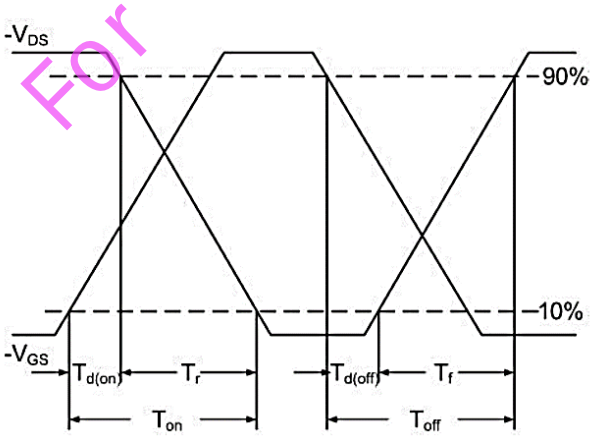


Fig.10 Switching Time Waveform

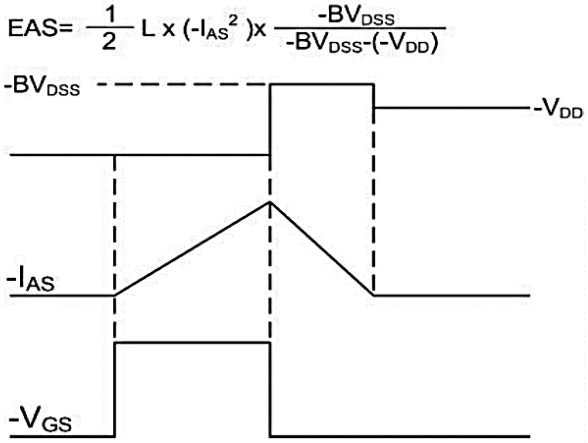
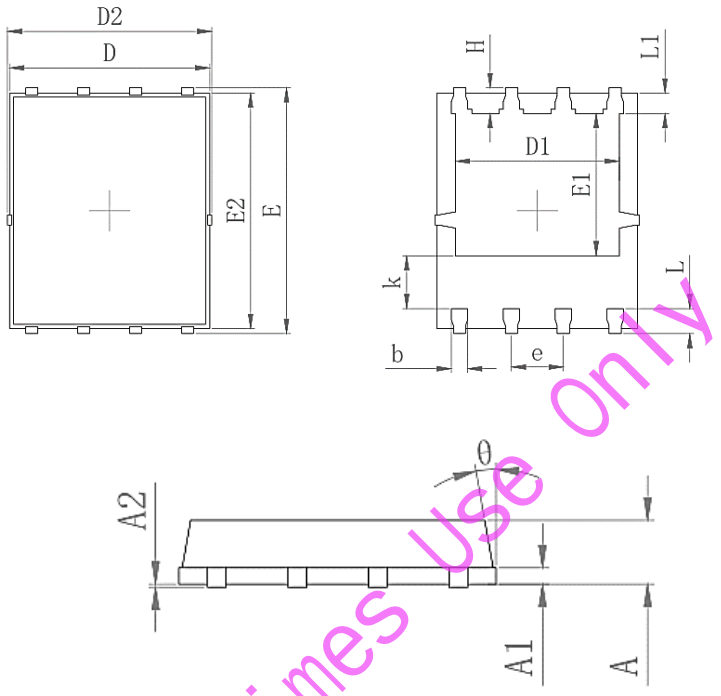


Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data-PDFN5*6-8L-JQ Single



Symbol	Common	
	mm	
	Mim	Max
A	0.900	1.100
A1	0.254	
A2	0-0.05	
D	4.824	4.976
D1	3.910	4.110
D2	4.944	5.076
E	5.924	6.076
E1	3.375	3.575
E2	5.674	5.826
b	0.350	0.450
e	1.270	
L	0.534	0.686
L1	0.424	0.576
K	1.190	1.390
H	0.549	0.701
	8°	12°

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30V P-Channel Enhancement Mode MOSFET

Edition	Date	Change
Rve1.0	2018/4/10	Initial release
Rve2.0	2019/10/10	Reduce RDS(on)
Rve2.1	2022/5/17	Correct package size