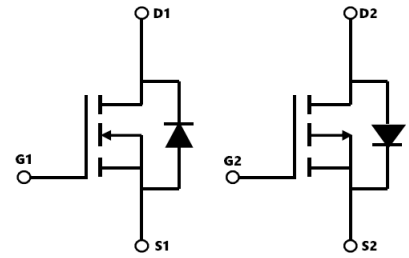


30V N+P-Channel Enhancement Mode MOSFET

Description

The AP20G03GD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.



General Features

$V_{DS} = 30V$ $I_D = 30A$

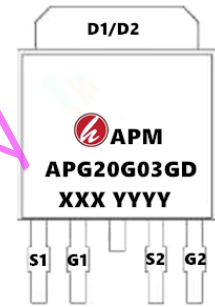
$R_{DS(ON)} < 22m\Omega$ @ $V_{GS}=10V$

$V_{DS} = -30V$ $I_D = -24A$

$R_{DS(ON)} < 35m\Omega$ @ $V_{GS}=10V$

Application

- Battery protection
- Load switch
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP20G03GD	TO-252-4L	AP20G03GD XXX YYYY	2500

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	30	-24	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	18	-19	A
I_{DM}	Pulsed Drain Current ²	60	-50	A
EAS	Single Pulse Avalanche Energy ³	22	45	mJ
I_{AS}	Avalanche Current	21	-30	A
$P_D @ T_C=25^\circ C$	Total Power Dissipation ⁴	25	25	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	5	$^\circ C/W$

30V N+P-Channel Enhancement Mode MOSFET**Electrical Characteristics (T_J=25°C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.0193	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =30A	---	15	22	mΩ
		V _{GS} =4.5V, I _D =15A	---	26	36	
V _{GS(th)}	Gate Threshold Voltage		1.2	---	2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient	V _{GS} =V _{DS} , I _D =250uA	---	-3.97	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =30A	---	34	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.8	---	Ω
Q _g	Total Gate Charge (4.5V)		---	9.8	---	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =15A	---	4.2	---	
Q _{gd}	Gate-Drain Charge		---	3.6	---	
T _{d(on)}	Turn-On Delay Time		---	4	---	ns
T _r	Rise Time	V _{DD} =15V, V _{GS} =10V, R _θ =3.3	---	8	---	
T _{d(off)}	Turn-Off Delay Time	I _D =15A	---	31	---	
T _f	Fall Time		---	4	---	
C _{iss}	Input Capacitance		---	940	---	pF
C _{oss}	Output Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	131	---	
C _{rss}	Reverse Transfer Capacitance		---	109	---	
I _S	Continuous Source Current ^{1,5}		---	---	43	A
I _{SM}	Pulsed Source Current ^{2,5}	V _G =V _D =0V, Force Current	---	---	112	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1	V
t _{rr}	Reverse Recovery Time	I _F =30A, di/dt=100A/μs	---	8.5	---	nS
Q _{rr}	Reverse Recovery Charge	T _J =25°C	---	2.2	---	nC

Note:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=21A
4. The power dissipation is limited by 150°C junction temperature 5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

N-Channel Typical Characteristics

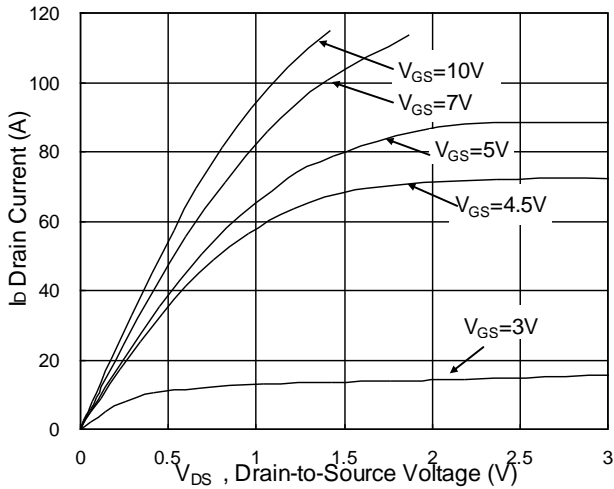


Fig.1 Typical Output Characteristics

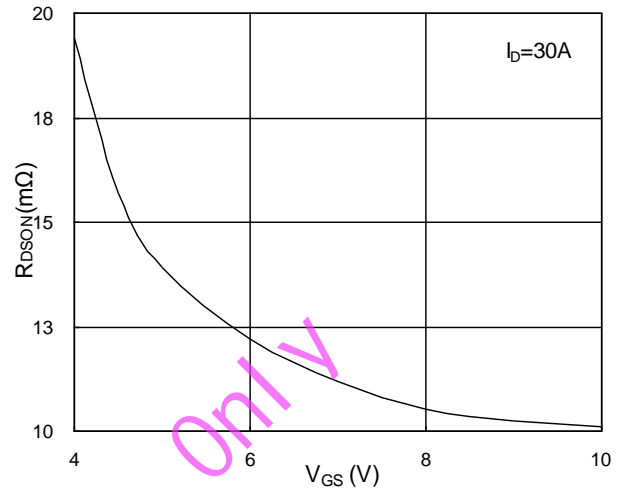


Fig.2 On-Resistance vs. G-S Voltage

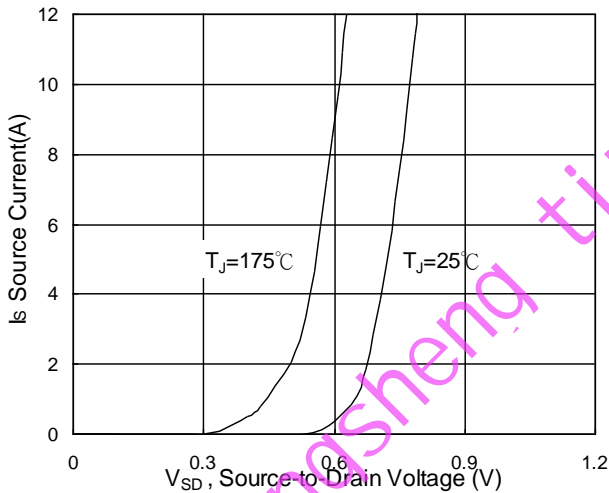


Fig.3 Forward Characteristics of Reverse

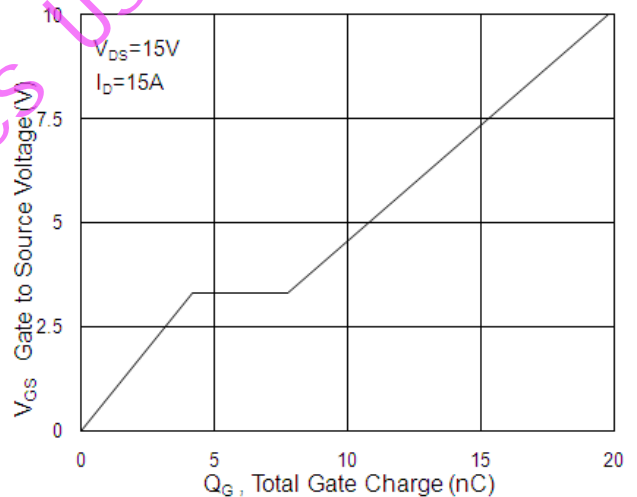


Fig.4 Gate-Charge Characteristics

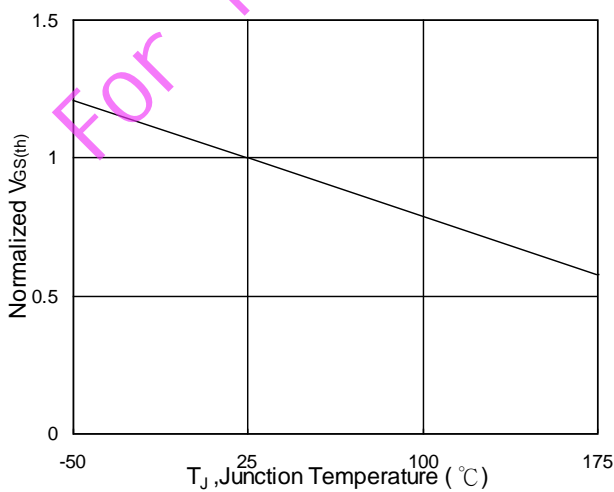


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

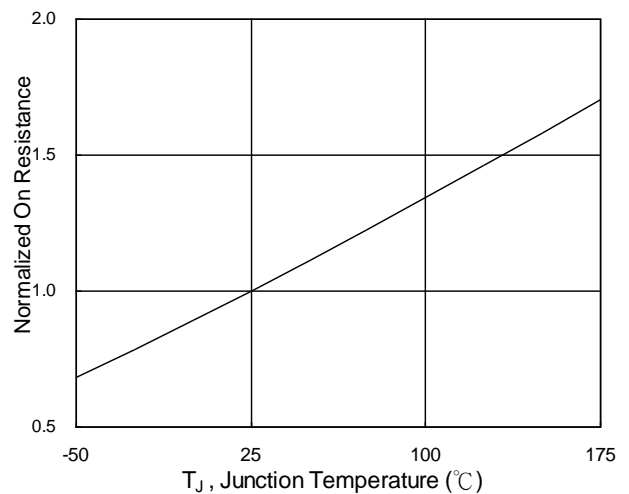


Fig.6 Normalized $R_{DS(on)}$ vs. T_J



30V N+P-Channel Enhancement Mode MOSFET

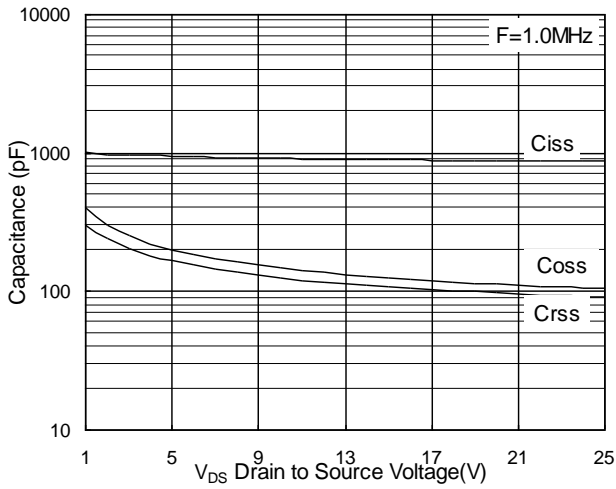


Fig.7 Capacitance

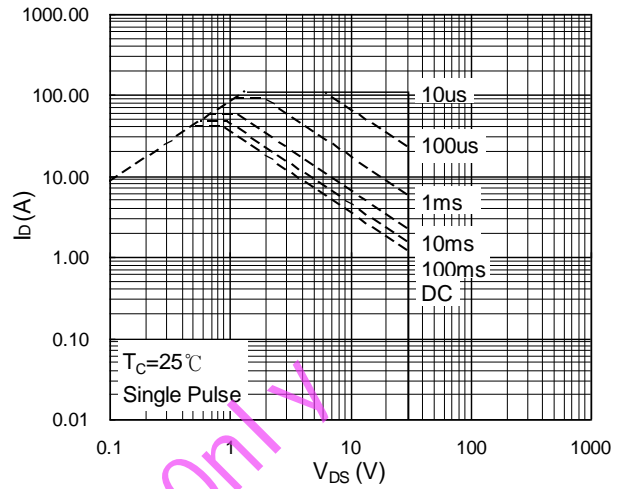


Fig.8 Safe Operating Area

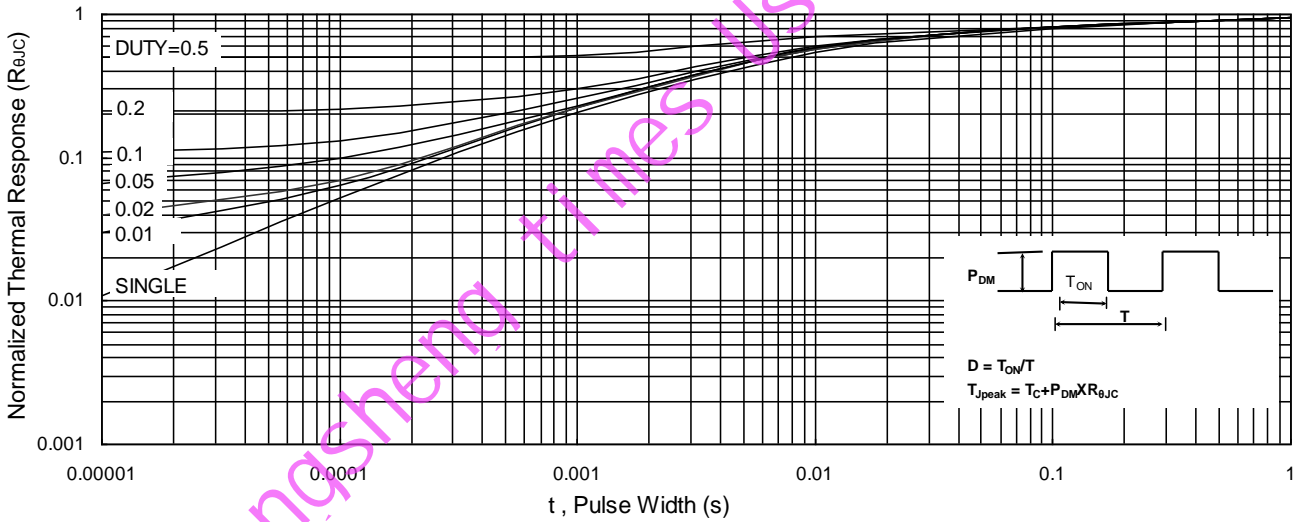


Fig.9 Normalized Maximum Transient Thermal Impedance

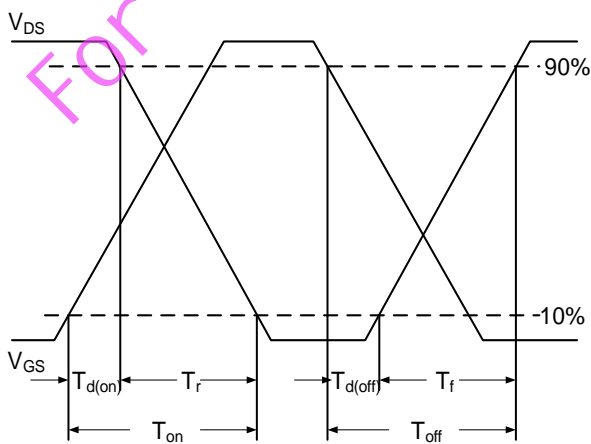


Fig.10 Switching Time Waveform

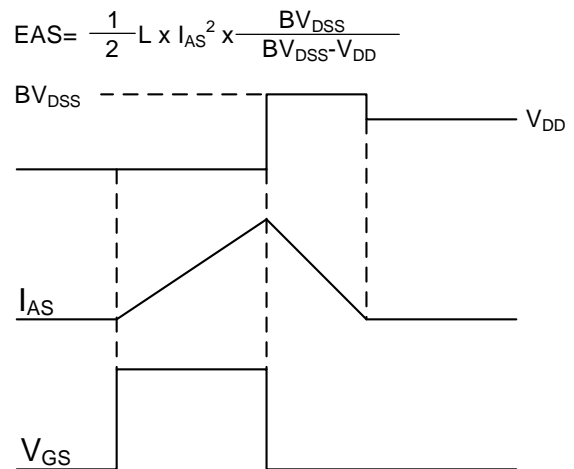


Fig.11 Unclamped Inductive Switching Waveform

30V N+P-Channel Enhancement Mode MOSFET**Electrical Characteristics (T_J=25°C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.021	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-12A	---	30	45	mΩ
		V _{GS} =-4.5V, I _D =-6A	---	38	55	
V _{GS(th)}	Gate Threshold Voltage		-1.0	-1.5	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient	V _{GS} =V _{DS} , I _D =-250uA	---	-4.2	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-12A	---	15	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		15	30	
Q _g	Total Gate Charge (-4.5V)		---	9.8	---	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-20V, V _{GS} =-4.5V, I _D =-12A	---	2.2	---	
Q _{gd}	Gate-Drain Charge		---	3.4	---	
T _{d(on)}	Turn-On Delay Time		---	16.4	---	ns
T _r	Rise Time	V _{DD} =-24V, V _{GS} =-10V, R _G =3.3Ω, I _D =-1A	---	20.2	---	
T _{d(off)}	Turn-Off Delay Time		---	55	---	
T _f	Fall Time		---	10	---	
C _{iss}	Input Capacitance		---	930	---	pF
C _{oss}	Output Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	148	---	
C _{rss}	Reverse Transfer Capacitance		---	115	---	
I _S	Continuous Source Current ^{1,5}		---	---	-24	A
I _{SM}	Pulsed Source Current ^{2,5}	V _G =V _D =0V, Force Current	---	---	-50	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rat.The power dissipation is limited by ing . The test condition is V_{150°C} junction temperature V_{DD}=-25 V, V_{GS}=-10V, L=0.1mH, I_{AS}=-30A
- 4
- 5 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

30V N+P-Channel Enhancement Mode MOSFET

P-Channel Typical Characteristics

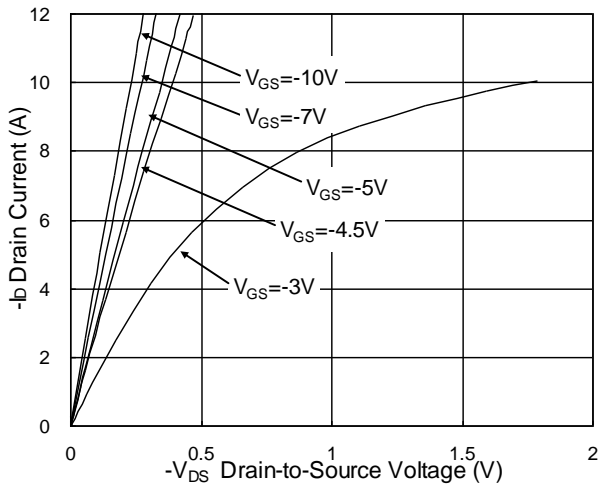


Fig.1 Typical Output Characteristics

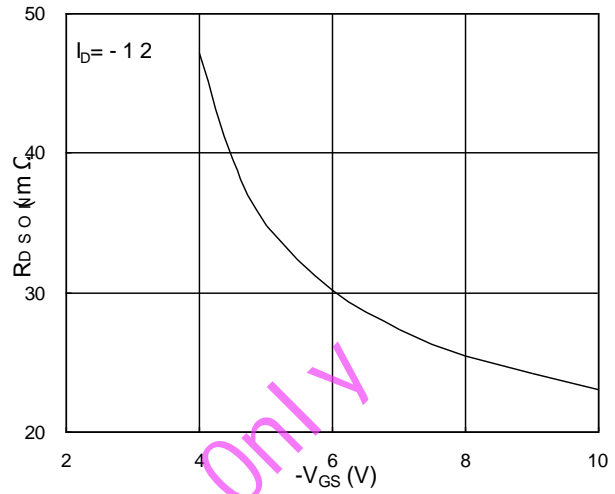


Fig.2 On-Resistance v.s Gate-Source

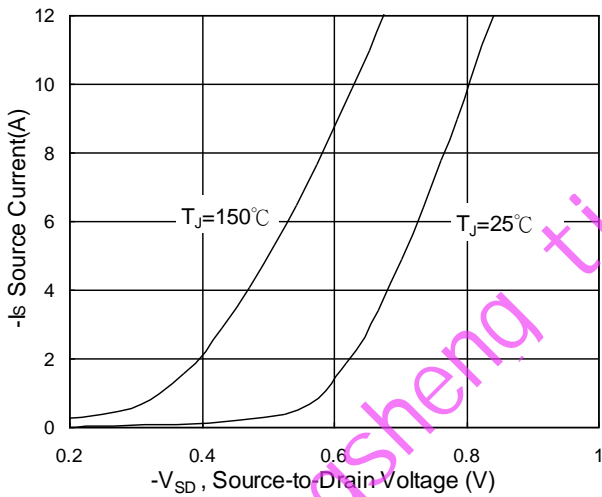


Fig.3 Forward Characteristics Of Reverse

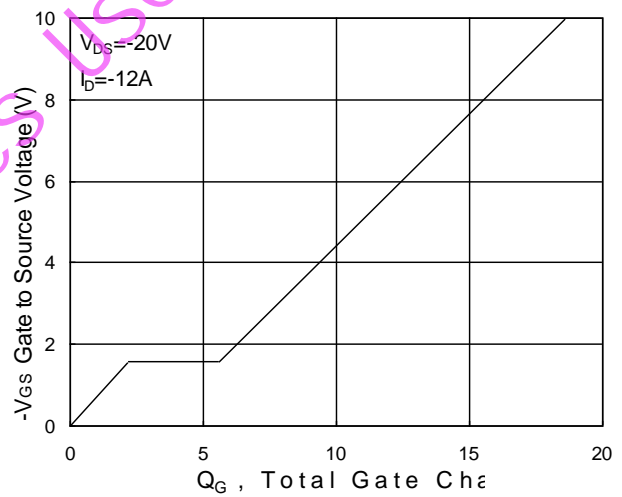


Fig.4 Gate-Charge Characteristics

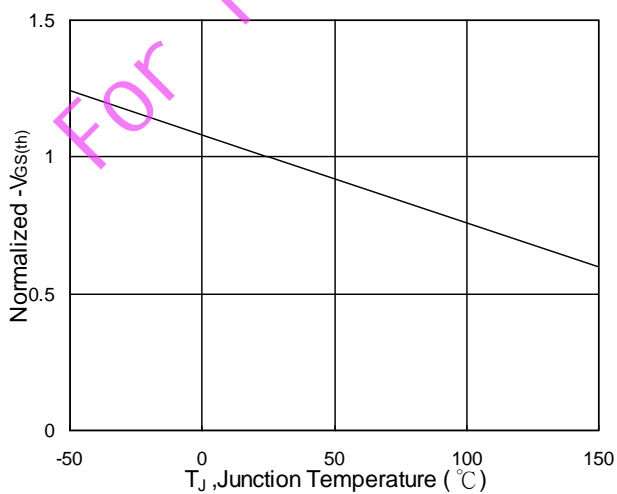


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

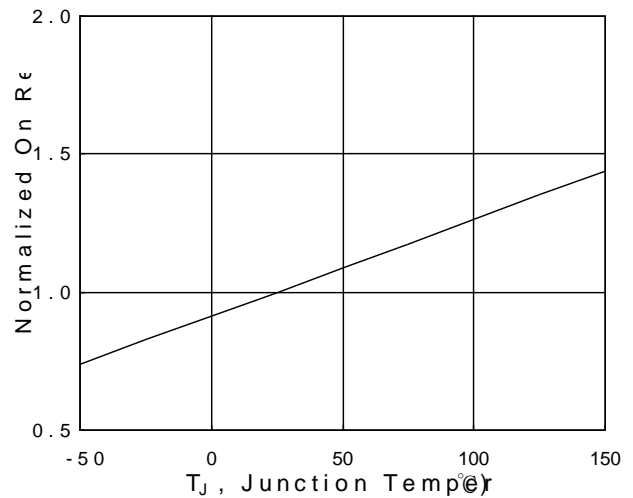


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

30V N+P-Channel Enhancement Mode MOSFET

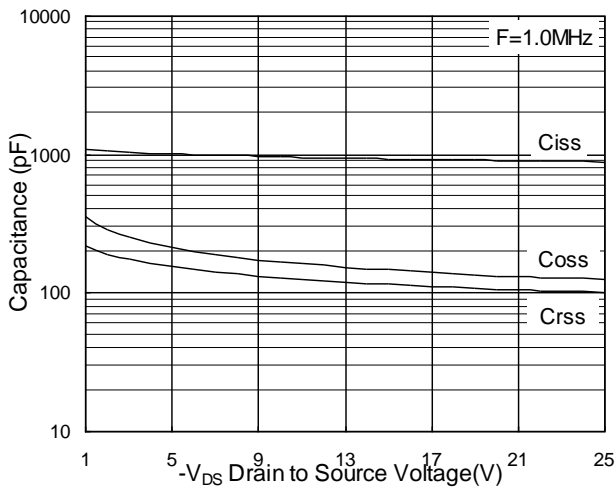


Fig.7 Capacitance

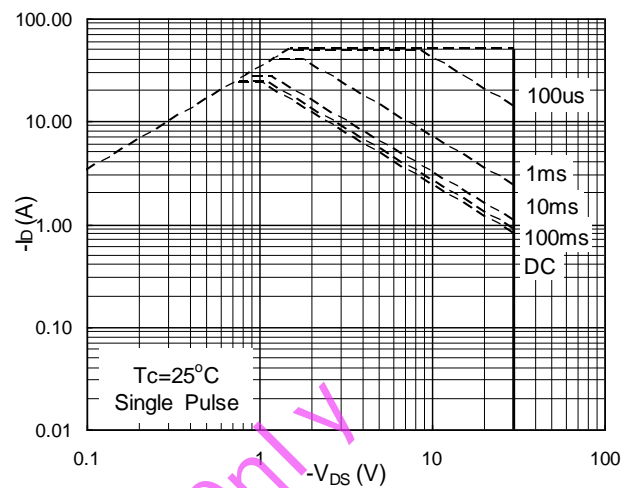


Fig.8 Safe Operating Area

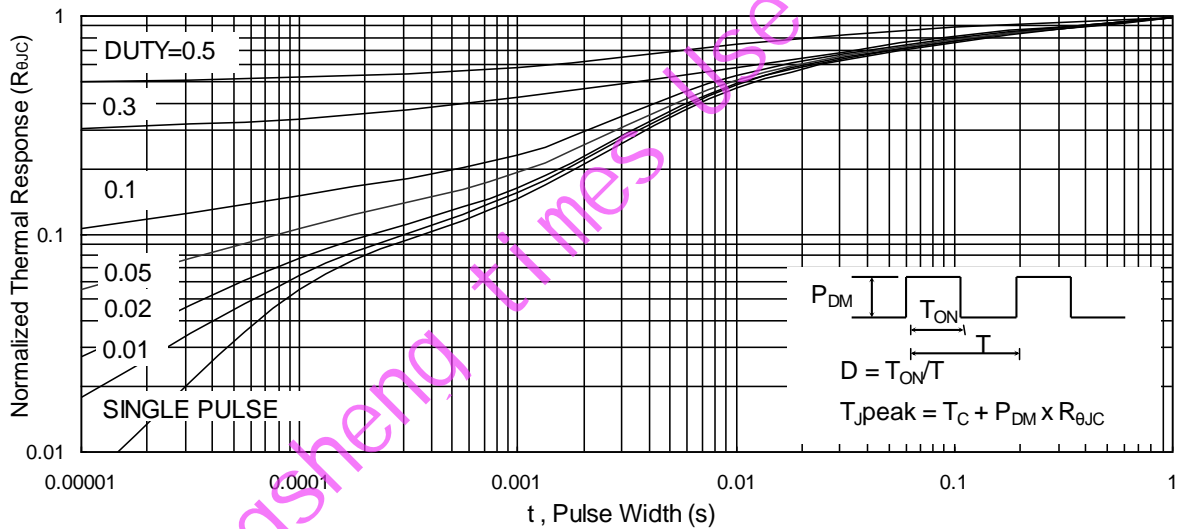


Fig.9 Normalized Maximum Transient Thermal Impedance

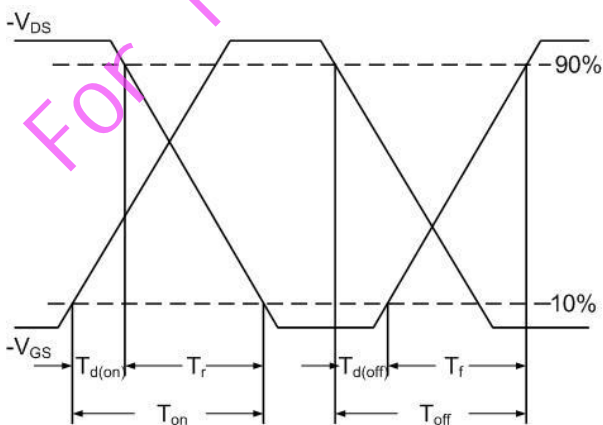


Fig.10 Switching Time Waveform

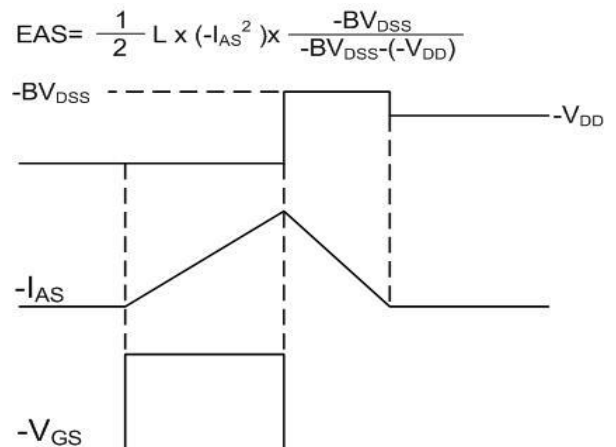
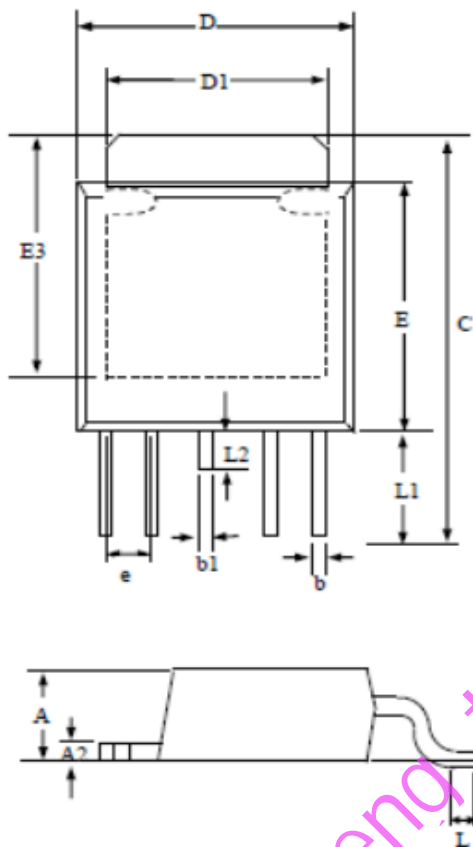


Fig.11 Unclamped Inductive Waveform



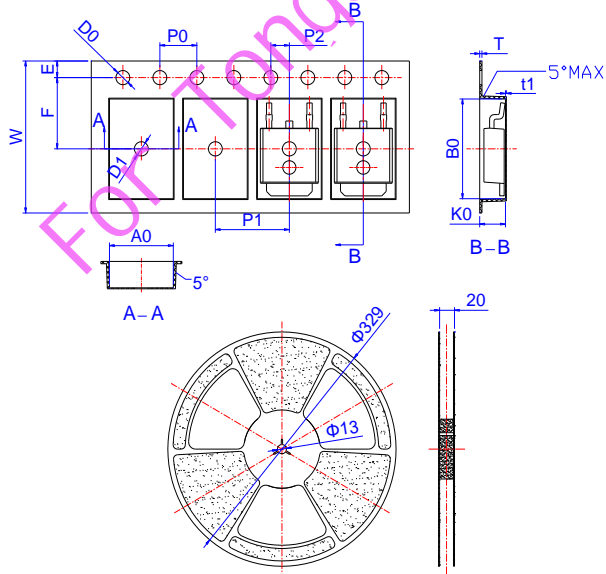
Package Mechanical Data



SYMBOLS	Millimeters		
	MIN	NOM	MAX
D	6.30	6.55	6.80
D1	4.80	5.35	5.90
C	9.30	9.75	10.20
E	5.30	5.80	6.30
E3	4.50	5.15	5.80
L	0.90	1.35	1.80
L1	2.00	2.53	3.05
L2	0.50	0.85	1.20
b	0.30	0.50	0.70
b1	0.40	0.60	0.80
A	2.10	2.30	2.50
A2	0.40	0.53	0.65
A1	0.00	0.10	0.20
e	1.20	1.30	1.40

1. All Dimensions Are in Millimeters.
2. Dimension Does Not Include Mold Protrusions.

Reel Specification-TO-252-4



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583

30V N+P-Channel Enhancement Mode MOSFET

Attention

- 1, Any and all APM Microelectronics products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your APM Microelectronics representative nearest you before using any APM Microelectronics products described or contained herein in such applications.
- 2, APM Microelectronics assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all APM Microelectronics products described or contained herein.
- 3, Specifications of any and all APM Microelectronics products described or contained here instipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- 4, APM Microelectronics Semiconductor CO., LTD. strives to supply high quality high reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- 5, In the event that any or all APM Microelectronics products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- 6, No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of APM Microelectronics Semiconductor CO., LTD.
- 7, Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. APM Microelectronics believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.
- 8, Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the APM Microelectronics product that you intend to use.