LM75A Digital Temperature Sensor and Thermal Watchdog With Two-Wire Interface

1 Features

- No External Components Required
- Shutdown Mode to Minimize Power Consumption
- Up to Eight LM75As can be Connected to a Single Bus
- Power up Defaults Permit Stand-Alone Operation as Thermostat
- Key Specifications:
  - Supply Voltage
    - LM75A: 2.7 V to 5.5 V
  - Supply Current
    - Operating: 280 µA (Typical)
    - Shutdown: 4 µA (Typical)
  - Temperature Accuracy
    - 25°C to 100°C: ±2°C (Max)
    - 55°C to 125°C: ±3°C (Max)

2 Applications

- General System Thermal Management
- Communications Infrastructure
- Electronic Test Equipment
- Environmental Monitoring

3 Description

The LM75A is an industry-standard digital temperature sensor with an integrated sigma-delta analog-to-digital converter (ADC) and I^2C interface. The LM75A provides 9-bit digital temperature readings with an accuracy of ±2°C from –25°C to 100°C and ±3°C over –55°C to 125°C.

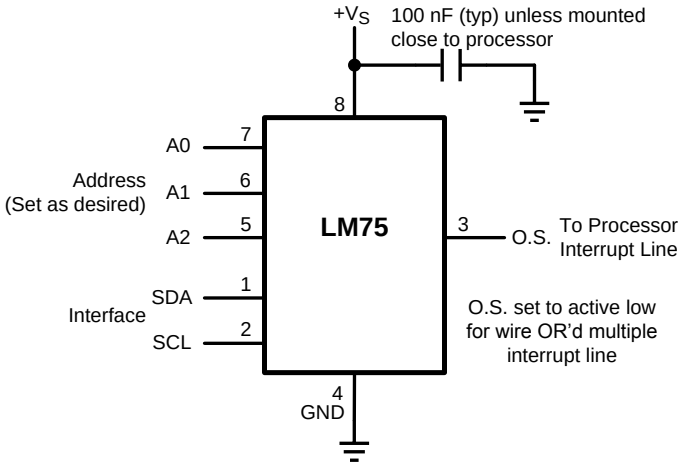
The LM75A operates with a single supply from 2.7 V to 5.5 V. Communication is accomplished over a 2-wire interface which operates up to 400 kHz. The LM75A has three address pins, allowing up to eight LM75A devices to operate on the same 2-wire bus. The LM75A has a dedicated overtemperature output (O.S.) with programmable limit and hysteresis. This output has programmable fault tolerance, which lets the user to define the number of consecutive error conditions that must occur before O.S. is activated. The wide temperature and supply range and I^2C interface make the LM75A ideal for a number of applications including base stations, electronic test equipment, office electronics, personal computers, and any other system in which thermal management is critical to performance. The LM75A is available in an SOIC-8 package and an VSSOP-8 package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM75A	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (May 2013) to Revision P **Page**

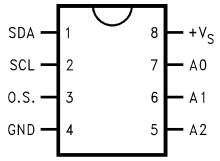
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision N (May 2013) to Revision O **Page**

- Changed layout of National Data Sheet to TI format ... 16

5 Pin Configuration and Functions

8-Pins
SOIC (D) and VSSOP (DGK) Packages
Top View



Pin Functions

PIN		DESCRIPTION	TYPICAL CONNECTION
NO.	NAME		
1	SDA	I^2C Serial Bi-Directional Data Line, Open Drain	From Controller, tied to a pullup resistor or current source
2	SCL	I^2C Clock Input	From Controller, tied to a pullup resistor or current source
3	O.S.	Overtemperature Shutdown, Open Drain Output	Pull–up Resistor, Controller Interrupt Line
4	GND	Power Supply Ground	Ground
5	A2	User-Set I^2C Address Inputs	Ground (Low, "0") or $+V_S$ (High, "1")
6	A1		
7	A0		
8	$+V_S$	Positive Supply Voltage Input	DC Voltage from 2.7 V to 5.5 V 100-nF bypass capacitor with 10-µF bulk capacitance in the near vicinity

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply Voltage Pin ($+V_S$)	−0.3	6.5	V
Voltage at A0, A1and A2 Pins	−0.3	($+V_S$ + 0.3) and must be ≤ 6.5	V
Voltage at OS, SCL and SDA Pins	−0.3	6.5	V
Input Current at any Pin(2)		5	mA
Package Input Current(2)		20	mA
O.S. Output Sink Current		10	mA
O.S. Output Voltage		6.5	V
Storage temperature, T_{stg}	–65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) When the input voltage (V_I) at any pin exceeds the power supplies (V_I < GND or V_I > $+V_S$) the current at that pin should be limited to 5mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5mA to four.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
	Machine model	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions(1)(2)

	MIN	MAX	UNIT
Specified Temperature Range (T_{MIN} to T_{MAX})	−55	125	°C
Supply Voltage Range (+V_S) LM75A	2.7	5.5	V

(1) LM75A θ_{JA} (thermal resistance, junction-to-ambient) when attached to a printed circuit board with 2 oz. foil similar to the one shown in Thermal Information is summarized in the table below the Operating Ratings table.
(2) Reflow temperature profiles are different for lead-free and non-lead-free packages. Soldering process must comply with *Reflow Temperature Profile* specifications. Refer to www.ti.com/packaging.(2)

6.4 Thermal Information

THERMAL METRIC(1)		LM75A		UNIT
		D	DGK	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	200	250	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for: +V_S = 2.7 to 5.5 Vdc for LM75AIM. T_A = T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
Accuracy		T_A = −25°C to +100°C –55°C ≤ T_J ≤ 125°C	–2		2	°C
		T_A = −55°C to +125°C –55°C ≤ T_J ≤ 125°C	–3		3	°C
Resolution				9		Bits
Temperature Conversion Time		See(3)		100		ms
		See(3), –55°C ≤ T_J ≤ 125°C			300	ms
Quiescent Current	LM75A	I^2C Inactive		0.28		mA
		I^2C Inactive, –55°C ≤ T_J ≤ 125°C			0.5	mA
		Shutdown Mode, +V_S = 3 V		4		µA
		Shutdown Mode, +V_S = 5 V		6		µA
O.S. Output Saturation Voltage		I_{OUT} = 4 mA, –55°C ≤ T_J ≤ 125°C			0.8	V
O.S. Delay		See(4), –55°C ≤ T_J ≤ 125°C	1		6	Conversion
T_{OS} Default Temperature		See(5)		80		°C
T_{HYST} Default Temperature		See(5)		75		°C

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.
(2) Maximum values (limits) are ensured to AOQL (Average Outgoing Quality Level).
(3) The conversion-time specification is provided to indicate how often the temperature data is updated. The LM75A can be accessed at any time and reading the Temperature Register will yield result from the last temperature conversion. When the LM75A is accessed, the conversion that is in process will be interrupted and it will be restarted after the end of the communication. Accessing the LM75A continuously without waiting at least one conversion time between communications will prevent the device from updating the Temperature Register with a new temperature conversion result. Consequently, the LM75A should not be accessed continuously with a wait time of less than 300ms.
(4) O.S. Delay is user programmable up to 6 “over limit” conversions before O.S. is set to minimize false tripping in noisy environments.
(5) Default values set at power up.

6.6 Digital DC Characteristics

Unless otherwise noted, these specifications apply for $+V_S$ = 2.7 to 5.5 Vdc for LM75AIM and LM75AIMM. $T_A = T_J$ = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
$V_{IN(1)}$	Logical “1” Input Voltage		–55°C ≤ T_J ≤ 125°C	+V_S × 0.7			V
						+V_S + 0.3	V
$V_{IN(0)}$	Logical “0” Input Voltage		–55°C ≤ T_J ≤ 125°C	−0.3			V
						+V_S × 0.3	V
$I_{IN(1)}$	Logical “1” Input Current		V_{IN} = +V_S		0.005		µA
			V_{IN} = +V_S, –55°C ≤ T_J ≤ 125°C			1.0	
$I_{IN(0)}$	Logical “0” Input Current		V_{IN} = 0 V		−0.005		µA
			V_{IN} = 0 V, –55°C ≤ T_J ≤ 125°C			−1.0	
C_{IN}	All Digital Inputs				5		pF
I_{OH}	High Level Output Current Open drain leakage	LM75A	V_{OH} = 5 V, –55°C ≤ T_J ≤ 125°C			1	µA
V_{OL}	Low Level Output Voltage		I_{OL} = 3 mA, –55°C ≤ T_J ≤ 125°C			0.4	V
t_{OF}	Output Fall Time		C_L = 400 pF I_O = 3 mA, –55°C ≤ T_J ≤ 125°C			250	ns

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.
(2) Maximum values (limits) are ensured to AOQL (Average Outgoing Quality Level).

6.7 I²C Digital Switching Characteristics

Unless otherwise noted, these specifications apply for $+V_S$ = 2.7 to 5.5 Vdc for LM75AIM and LM75AIMM on output lines = 80 pF unless otherwise specified. $T_A = T_J$ = 25°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX(2)(3)	UNIT
t_1	SCL (Clock) Period		–55°C ≤ T_J ≤ 125°C	2.5			ns
t_2	Data in Set-Up Time to SCL High		–55°C ≤ T_J ≤ 125°C	100			ns
t_3	Data Out Stable after SCL Low		–55°C ≤ T_J ≤ 125°C	0			ns
t_4	SDA Low Set-Up Time to SCL Low (Start Condition)		–55°C ≤ T_J ≤ 125°C	100			ns
t_5	SDA High Hold Time after SCL High (Stop Condition)		–55°C ≤ T_J ≤ 125°C	100			ns
$t_{TIMEOUT}$	SDA Time Low for Reset of Serial Interface(4)	LM75A		75			ms
			–55°C ≤ T_J ≤ 125°C			325	

(1) Typicals are at T_A = 25°C and represent most likely parametric norm.
(2) Maximum values (limits) are ensured to AOQL (Average Outgoing Quality Level).
(3) Timing specifications are tested at the bus input logic levels (Vin(0)=0.3XVA for a falling edge and Vin(1)=0.7XVA for a rising edge) when the SCL and SDA edge rates are similar.
(4) Holding the SDA line low for a time greater than $t_{TIMEOUT}$ will cause the LM75A to reset SDA to the IDLE state of the serial bus communication (SDA set High).

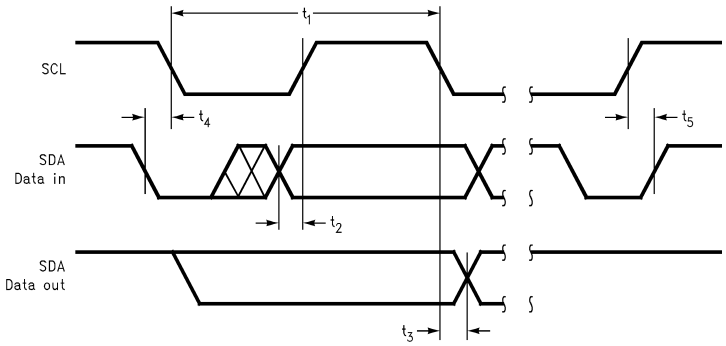


Figure 1. Timing Diagram

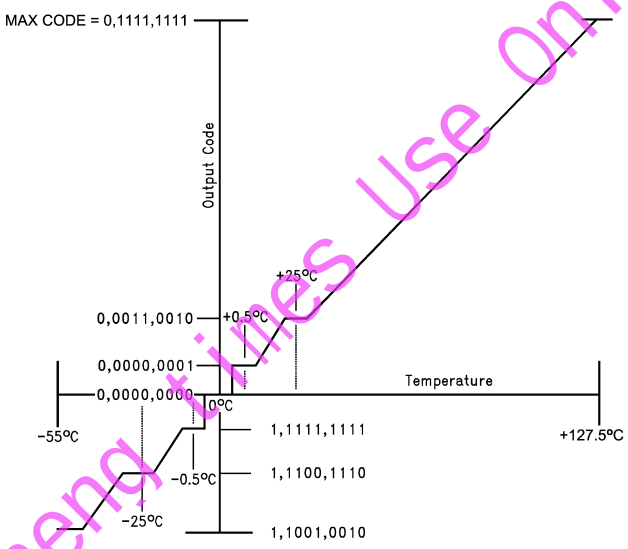


Figure 2. Temperature-to-Digital Transfer Function (Non-Linear Scale for Clarity)

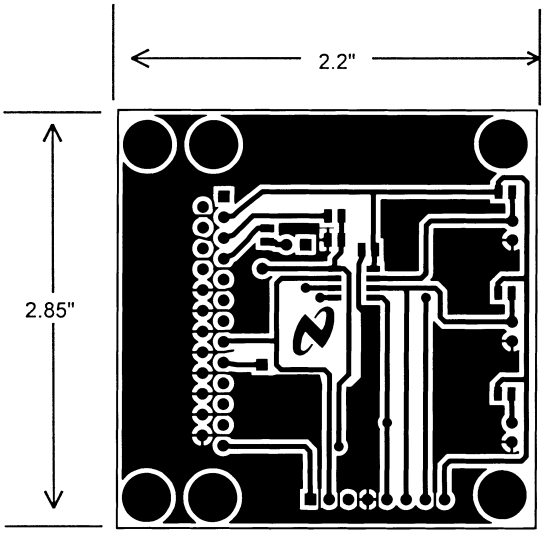
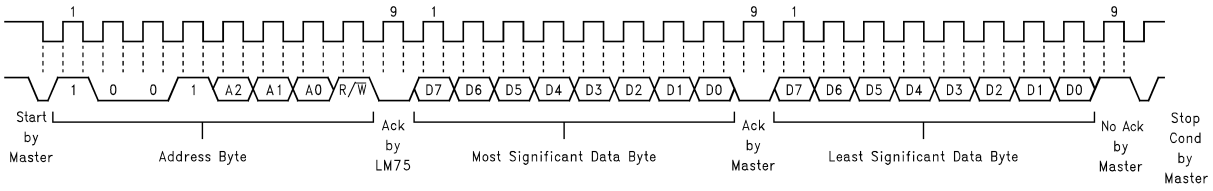
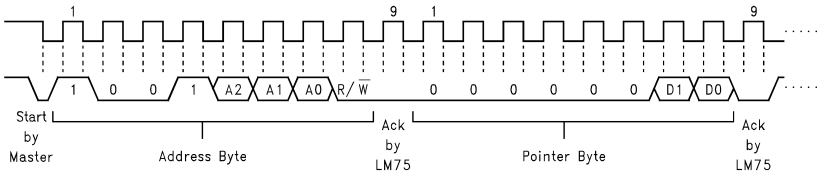
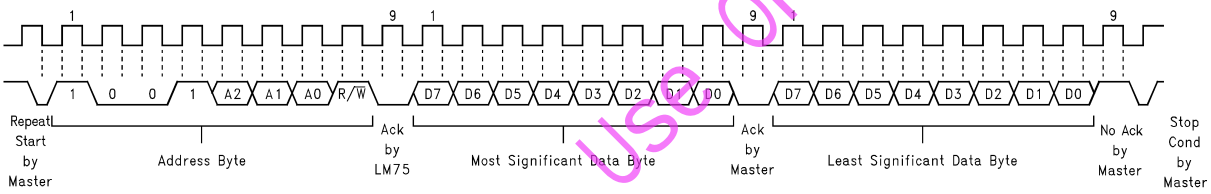


Figure 3. Printed Circuit Board Used for Thermal Resistance Specifications

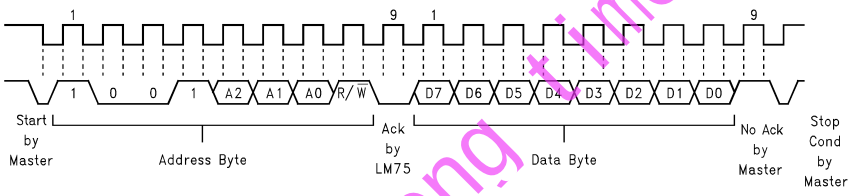


(a) Typical 2−Byte Read From Preset Pointer Location Such as Temp, T_{OS}, T_{HYST}



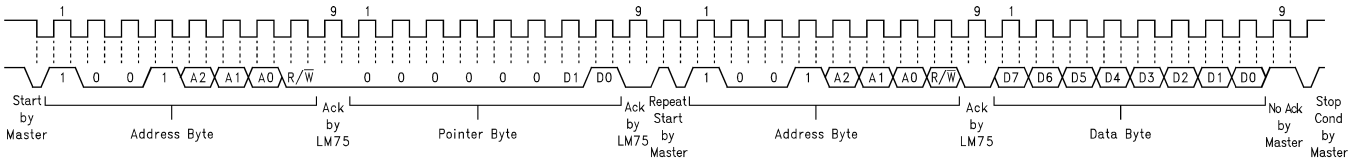


(b) Typical Pointer Set Followed by Immediate Read for 2−Byte Register such as Temp, T_{OS}, T_{HYST}

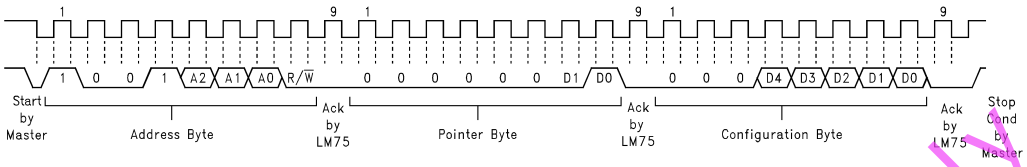


(c) Typical 1−Byte Read From Configuration Register With Preset Pointer

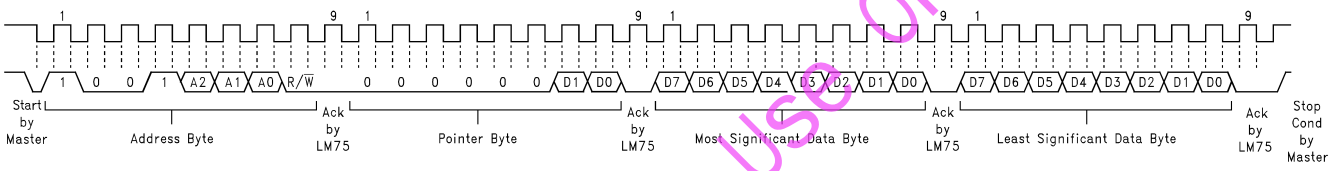
Figure 4. I^2C Timing Diagram



(a) Typical Pointer Set Followed by Immediate Read from Configuration Register



(b) Configuration Register Write



(c) T_{OS} and T_{HYST} Write

Figure 5. I²C Timing Diagrams (Continued)

6.8 Typical Characteristics

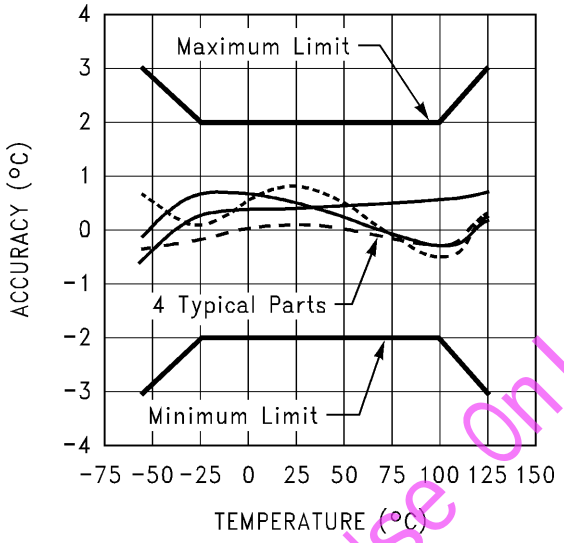


Figure 6. Accuracy vs Temperature (LM75A)

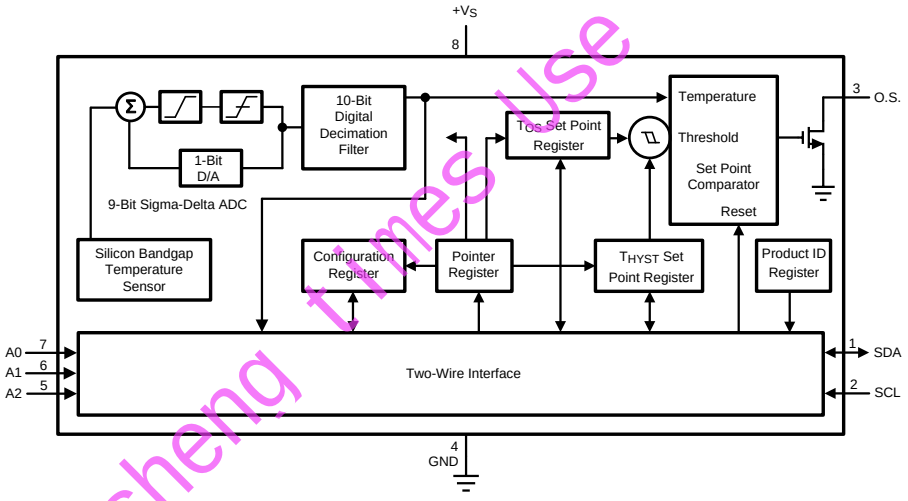
7 Detailed Description

7.1 Overview

The LM75A temperature sensor incorporates a band-gap type temperature sensor and 9-bit ADC (sigma-delta ADC). The temperature data output of the LM75A is available at all times via the I^2C bus. If a conversion is in progress, it will be stopped and restarted after the read. A digital comparator is also incorporated that compares a series of readings, the number of which is user-selectable, to user-programmable setpoint and hysteresis values. The comparator trips the O.S. output line, which is programmable for mode and polarity. The LM75A has an integrated low-pass filter on both the SDA and the SCL line. These filters increase communications reliability in noisy environments.

The LM75A also has a bus fault timeout feature. If the SDA line is held low for longer than $t_{TIMEOUT}$ (see specification) the LM75A will reset to the IDLE state (SDA set to high impedance) and wait for a new start condition. The TIMEOUT feature is not functional in Shutdown Mode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Digital Temperature Sensor

The LM75A is an industry-standard digital temperature sensor with an integrated sigma-delta ADC and I^2C interface. The LM75A provides 9-bit digital temperature readings with an accuracy of ±2°C from –25°C to 100°C and ±3°C over –55°C to 125°C.

The LM75A operates with a single supply from +2.7 V to +5.5 V. Communication is accomplished over a 2-wire interface which operates up to 400kHz. The LM75A has three address pins, allowing up to eight LM75A devices to operate on the same 2-wire bus. The LM75A has a dedicated over-temperature output (O.S.) with programmable limit and hysteresis. This output has programmable fault tolerance, which allows the user to define the number of consecutive error conditions that must occur before O.S. is activated.

7.4 Device Functional Modes

In Comparator mode the O.S. Output behaves like a thermostat. The output becomes active when temperature exceeds the T_{OS} limit, and leaves the active state when the temperature drops below the T_{HYST} limit. In this mode the O.S. output can be used to turn a cooling fan on, initiate an emergency system shutdown, or reduce system clock speed. Shutdown mode does not reset O.S. state in a comparator mode.

In Interrupt mode exceeding T_{OS} also makes O.S. active but O.S. will remain active indefinitely until reset by reading any register via the I^2C interface. Once O.S. has been activated by crossing T_{OS}, then reset, it can be activated again only by Temperature going below T_{HYST}. Again, it will remain active indefinitely until being reset by a read. Placing the LM75A in shutdown mode also resets the O.S. Output.

Device Functional Modes (continued)

The LM75A always powers up in a known state. The power up default conditions are:

- Comparator mode
- T_{OS} = 80°C
- T_{HYST} = 75°C
- O.S. active low
- Pointer = “00”

When the supply voltage is less than about 1.7V, the LM75A is considered powered down. As the supply voltage rises above the nominal 1.7V power up threshold, the internal registers are reset to the power up default values listed above.

If the LM75A is *not connected* to the I^2C bus on power up, it will act as a stand-alone thermostat with the power up default conditions listed above. It is optional, but recommended, to connect the address pins (A2, A1, A0) and the SCL and SDA pins together and to a 10k pullup resistor to $+V_S$ for better noise immunity. Any of these pins may also be tied high separately through a 10-k pullup resistor.

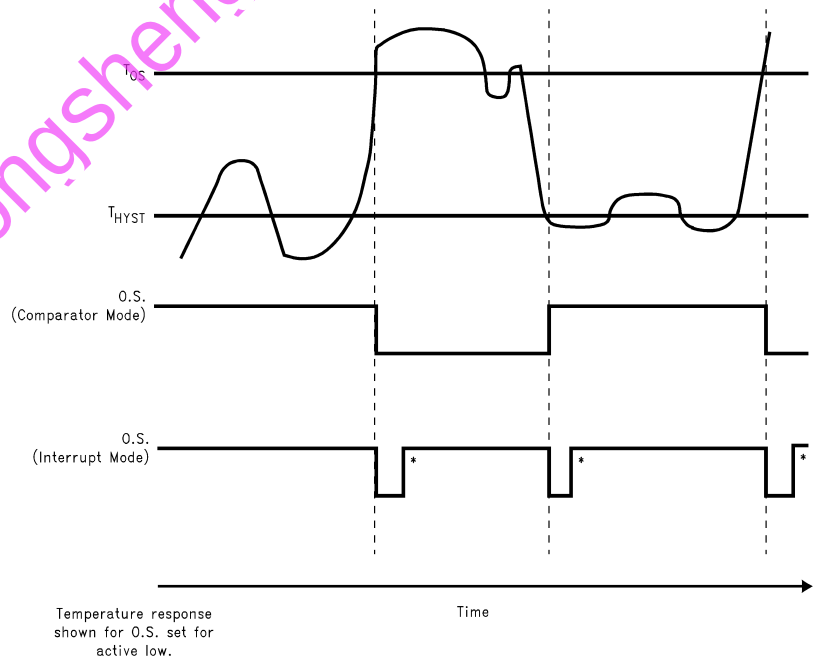
7.5 Programming

7.5.1 I^2C Bus Interface

The LM75A operates as a slave on the I^2C bus, so the SCL line is an input (no clock is generated by the LM75A) and the SDA line is a bi-directional serial data path. According to I^2C bus specifications, the LM75A has a 7-bit slave address. The four most significant bits of the slave address are hard wired inside the LM75A and are “1001”. The three least significant bits of the address are assigned to pins A2–A0, and are set by connecting these pins to ground for a low, (0); or to $+V_S$ for a high, (1).

Therefore, the complete slave address is:

1	0	0	1	A2	A1	A0
MSB						LSB



These interrupt mode resets of O.S. occur only when LM75A is read or placed in shutdown. Otherwise, O.S. would remain active indefinitely for any event.

Figure 7. O.S. Output Temperature Response Diagram

7.5.2 Temperature Data Format

Temperature data can be read from the Temperature, T_{OS} Set Point, and T_{HYST} Set Point registers; and written to the T_{OS} Set Point, and T_{HYST} Set Point registers. Temperature data is represented by a 9-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.5°C:

Temperature	Digital Output	
	Binary	Hex
+125°C	0 1111 1010	0FAh
+25°C	0 0011 0010	032h
+0.5°C	0 0000 0001	001h
0°C	0 0000 0000	000h
−0.5°C	1 1111 1111	1FFh
−25°C	1 1100 1110	1CEh
−55°C	1 1001 0010	192h

7.5.3 Shutdown Mode

Shutdown mode is enabled by setting the shutdown bit in the Configuration register via the I^2C bus. Shutdown mode reduces power supply current significantly. See specified quiescent current specification in the electrical tables. In Interrupt mode O.S. is reset if previously set and is undefined in Comparator mode during shutdown. The I^2C interface remains active. Activity on the clock and data lines of the I^2C bus may slightly increase shutdown mode quiescent current. T_{OS}, T_{HYST}, and Configuration registers can be read from and written to in shutdown mode.

For the LM75A, the TIMEOUT feature is turned off in Shutdown Mode.

7.5.4 Fault Queue

A fault queue of up to 6 faults is provided to prevent false tripping of O.S. when the LM75A is used in noisy environments. The number of faults set in the queue must occur consecutively to set the O.S. output.

7.5.5 Comparator and Interrupt Mode

As indicated in the O.S. Output Temperature Response Diagram, Figure 7, the events that trigger O.S. are identical for either Comparator or Interrupt mode. The most important difference is that in Interrupt mode the O.S. will remain set indefinitely once it has been set. To reset O.S. while in Interrupt mode, perform a read from any register in the LM75A.

7.5.6 O.S. Output

The O.S. output is an open-drain output and does not have an internal pullup. A “high” level will not be observed on this pin until pullup current is provided from some external source, typically a pullup resistor. Choice of resistor value depends on many system factors but, in general, the pullup resistor should be as large as possible. This will minimize any errors due to internal heating of the LM75A. The maximum resistance of the pullup, based on LM75A specification for High Level Output Current, to provide a 2-V high level, is 30 kΩ.

7.5.7 O.S. Polarity

The O.S. output can be programmed via the configuration register to be either active low (default mode), or active high. In active low mode the O.S. output goes low when triggered exactly as shown on the O.S. Output Temperature Response Diagram, Figure 7. Active high simply inverts the polarity of the O.S. output.

7.5.8 Internal Register Structure

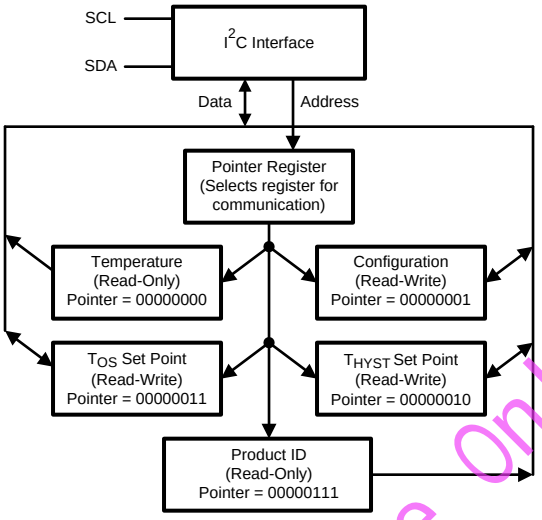


Figure 8. Register Structure

There are four data registers in the LM75A and an additional Product ID register selected by the Pointer register. At power-up the Pointer is set to "000"; the location for the Temperature Register. The Pointer register latches whatever the last location it was set to. In Interrupt Mode, a read from the LM75A, or placing the device in shutdown mode, resets the O.S. output. All registers are read and write, except the Temperature register and the LM75A's Product ID register, which are read-only.

A write to the LM75A will always include the address byte and the Pointer byte. A write to the Configuration register requires one data byte, and the T_{OS} and T_{HYST} registers require two data bytes.

Reading the LM75A can take place either of two ways: If the location latched in the Pointer is correct (most of the time it is expected that the Pointer will point to the Temperature register because it will be the data most frequently read from the LM75A), then the read can simply consist of an address byte, followed by retrieving the corresponding number of data bytes. If the Pointer needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a read.

The first data byte is the most significant byte with most significant bit first, permitting only as much data as necessary to be read to determine temperature condition. For instance, if the first four bits of the temperature data indicates an overtemperature condition, the host processor could immediately take action to remedy the excessive temperatures. At the end of a read, the LM75A can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

7.6 Register Maps

7.6.1 Pointer Register (Selects Which Registers Will Be Read From or Written to):

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	Register Select		

P0-P1: Register Select:

P2	P1	P0	Register
0	0	0	Temperature (Read-only) (Power-up default)
0	0	1	Configuration (Read/Write)
0	1	0	T_{HYST} (Read/Write)
0	1	1	T_{OS} (Read/Write)
1	1	1	Product ID Register

P3–P7: Must be kept zero.

7.6.2 Temperature Register (Read-Only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB	X	X	X	X	X	X	X

D0–D6: Undefined. D7–D15: Temperature Data. One LSB = 0.5°C. Two's complement format.

7.6.3 Configuration Register (Read/Write):

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Fault Queue		O.S. Polarity	Cmp/Int	Shutdown

Power up default is with all bits “0” (zero).

D0: Shutdown: When set to 1 the LM75A goes to low power shutdown mode.

D1: Comparator/Interrupt mode: 0 is Comparator mode, 1 is Interrupt mode.

D2: O.S. Polarity: 0 is active low, 1 is active high. O.S. is an open-drain output under all conditions.

D3–D4: Fault Queue: Number of faults necessary to detect before setting O.S. output to avoid false tripping due to noise. Faults are determine at the end of a conversion. See specified temperature conversion time in the electrical tables.

D4	D3	Number of Faults
0	0	1 (Power-up default)
0	1	2
1	0	4
1	1	6

D5–D7: These bits are used for production testing and must be kept zero for normal operation.

7.6.4 T_{HYST} and T_{OS} Register (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MSB	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB	X	X	X	X	X	X	X

D0–D6: Undefined D7–D15: T_{HYST} Or T_{OS} Trip Temperature Data. Power up default is T_{OS} = 80°C, T_{HYST} = 75°C

7.6.5 PRODID: Product ID Register (Read-Only) Pointer Address: 07h

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	0	0	1

D4--D7 Product Identification Nibble. Always returns Ah to uniquely identify this part as the LM75A.

D0--D3 Die Revision Nibble. Returns 1h to uniquely identify the revision level as one.

8 Application and Implementation

NOTE

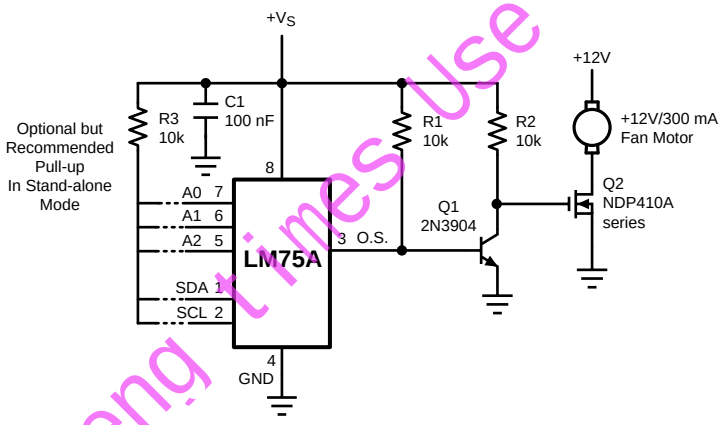
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The wide temperature and supply range and I^2C interface make the LM75A ideal for a number of applications including base stations, electronic test equipment, office electronics, personal computers, and any other system where thermal management is critical to performance.

8.2 Typical Applications

8.2.1 Simple Fan Controller, Interface Optional



When using the two-wire interface: program O.S. for active high and connect O.S. directly to Q2's gate.

Figure 9. Simple Fan Controller, Interface Optional

8.2.1.1 Design Requirements

The LM75A requires positive supply voltage of 2.7 V to 5.5 V to be applied between +Vs and GND. For best results, bypass capacitors of 100 nF and 10 µF are recommended. Pullup resistors of 10 kΩ are required on SCL and SDA.

8.2.1.2 Detailed Design Procedure

Accessing the conversion result of the LM75A consists of writing an address byte followed by retrieving the corresponding number of data bytes. The first data byte is the most significant byte with the most significant bit first, permitting only as much data as necessary to be read to determine temperature condition. For instance, if the first four bits of the temperature data indicates an overtemperature condition, the host processor could immediately take action to remedy the excessive temperatures. At the end of a read, the LM75A can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte). Temperature data is two's complement format and one LSB is equivalent to 0.5°C.

Typical Applications (continued)

8.2.1.3 Application Curve

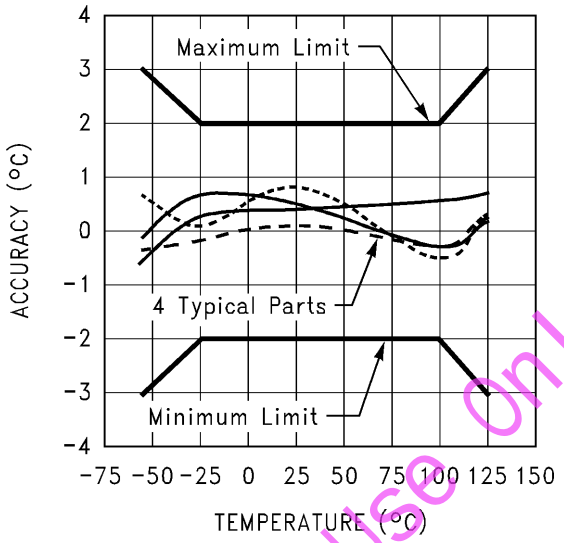


Figure 10. Temperature Accuracy

8.3 System Examples

8.3.1 Simple Thermostat, Interface Optional

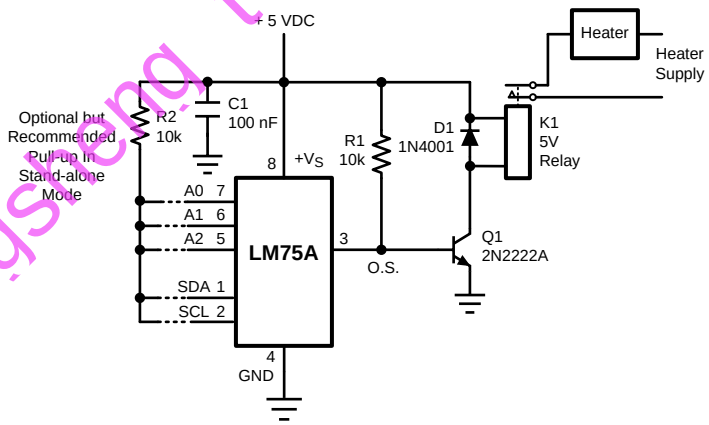


Figure 11. Simple Thermostat, Interface Optional

System Examples (continued)

8.3.2 Temperature Sensor with Loudmouth Alarm (Barking Watchdog)

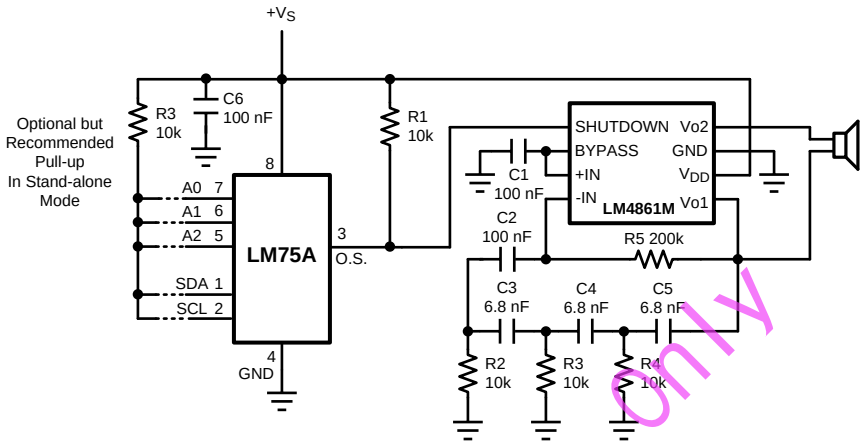


Figure 12. Temperature Sensor with Loudmouth Alarm (Barking Watchdog)

9 Power Supply Recommendations

The LM75A is specified for operation from 2.7 V to 5.5 V. Place 100-nF and 10-µF capacitors close to +Vs in order to reduce errors coupling in from noisy or high impedance supplies.

10 Layout

10.1 Layout Guidelines

To achieve the expected results when measuring temperature with an integrated circuit temperature sensor like the LM75A, it is important to understand that the sensor measures its own die temperature. For the LM75A, the best thermal path between the die and the outside world is through the LM75A's pins. In the VSSOP-8 package, the GND pin is directly connected to the die, so the GND pin provides the best thermal path. If the other pins are at different temperatures (unlikely, but possible), they will affect the die temperature, but not as strongly as the GND pin. In the SOIC-8 package, none of the pins is directly connected to the die, so they will all contribute similarly to the die temperature. Because the pins represent a good thermal path to the LM75A die, the LM75A will provide an accurate measurement of the temperature of the printed circuit board on which it is mounted. There is a less efficient thermal path between the plastic package and the LM75A die. If the ambient air temperature is significantly different from the printed circuit board temperature, it will have a small effect on the measured temperature.

In probe-type applications, the LM75A can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM75A and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM75A or its connections.

10.1.1 Digital Noise Issues

The LM75A features an integrated low-pass filter on both the SCL and the SDA digital lines to mitigate the effects of bus noise. Although this filtering makes the LM75A communication robust in noisy environments, good layout practices are always recommended. Minimize noise coupling by keeping digital traces away from switching power supplies. Also, ensure that digital lines containing high-speed data communications cross at right angles to the SDA and SCL lines. Excessive noise coupling into the SDA and SCL lines on the LM75A—specifically noise with amplitude greater than 400 mV_{pp} (the LM75A's typical hysteresis), overshoot greater than 300mV above +Vs, and undershoot more than 300 mV below GND—may prevent successful serial communication with the LM75A. Serial bus no-acknowledge is the most common symptom, causing unnecessary traffic on the bus. Although the serial bus maximum frequency of communication is only 400 kHz, care must be taken to ensure proper termination within a system with long printed circuit board traces or multiple parts on the bus.

10.2 Layout Example

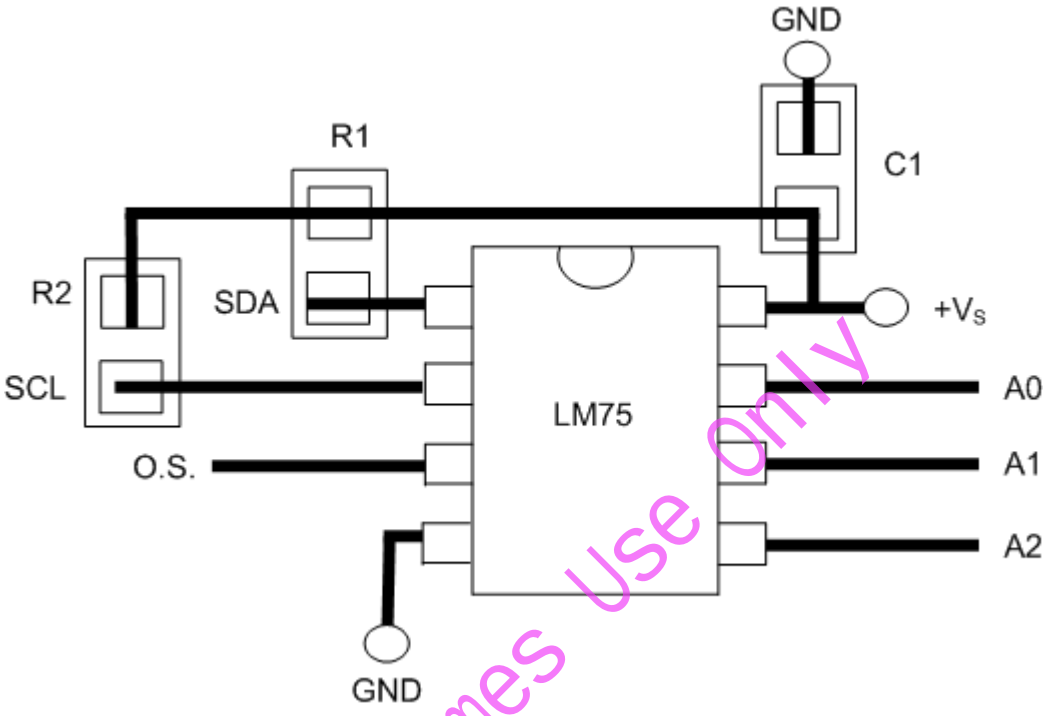


Figure 13. Printed Circuit Board Used for Thermal Resistance Specifications

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM75AIM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	LM75 AIM	Samples
LM75AIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	T00A	Samples
LM75AIMME/NOPB	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	T00A	Samples
LM75AIMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	T00A	Samples
LM75AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 125	LM75 AIM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

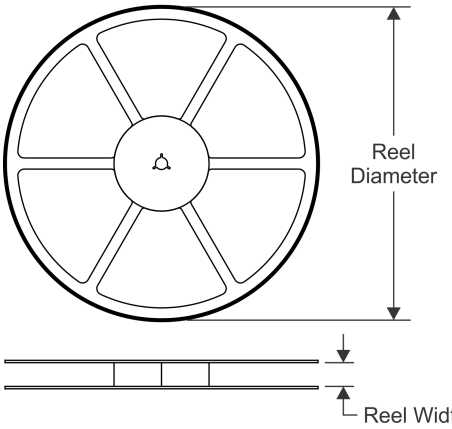
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

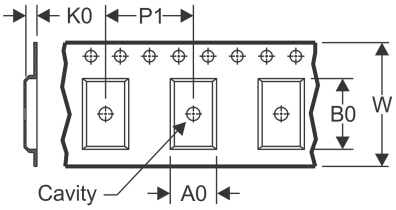
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

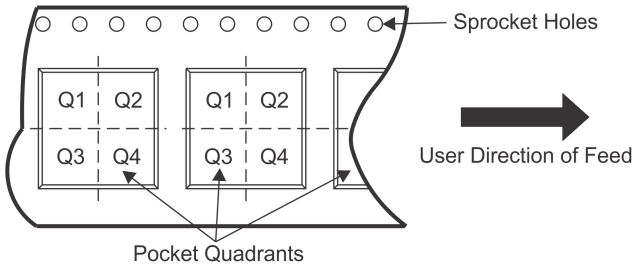


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

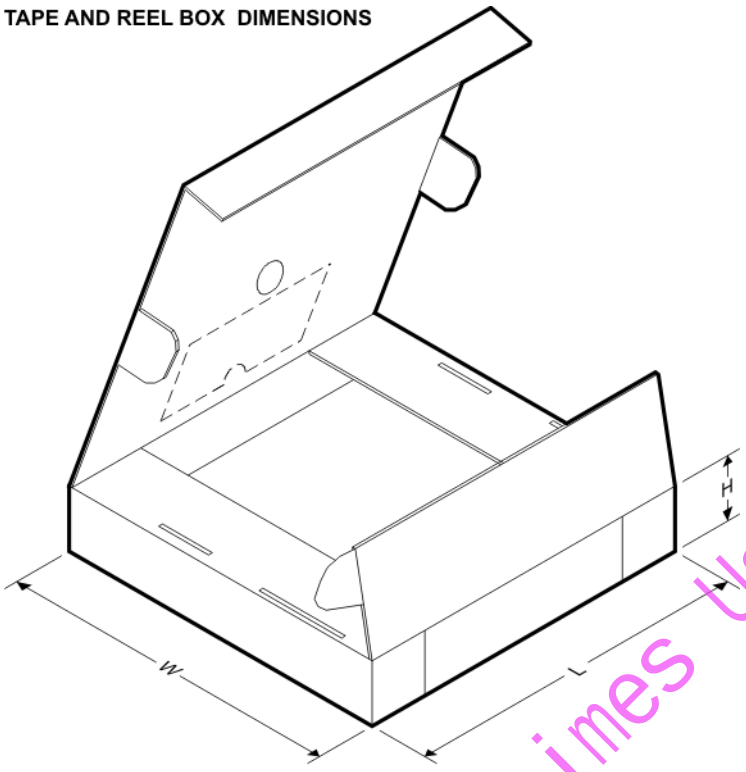
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

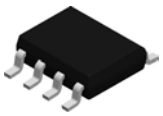
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM75AIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM75AIMME/NOPB	VSSOP	DGK	8	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM75AIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM75AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM75AIMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM75AIMME/NOPB	VSSOP	DGK	8	250	208.0	191.0	35.0
LM75AIMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM75AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

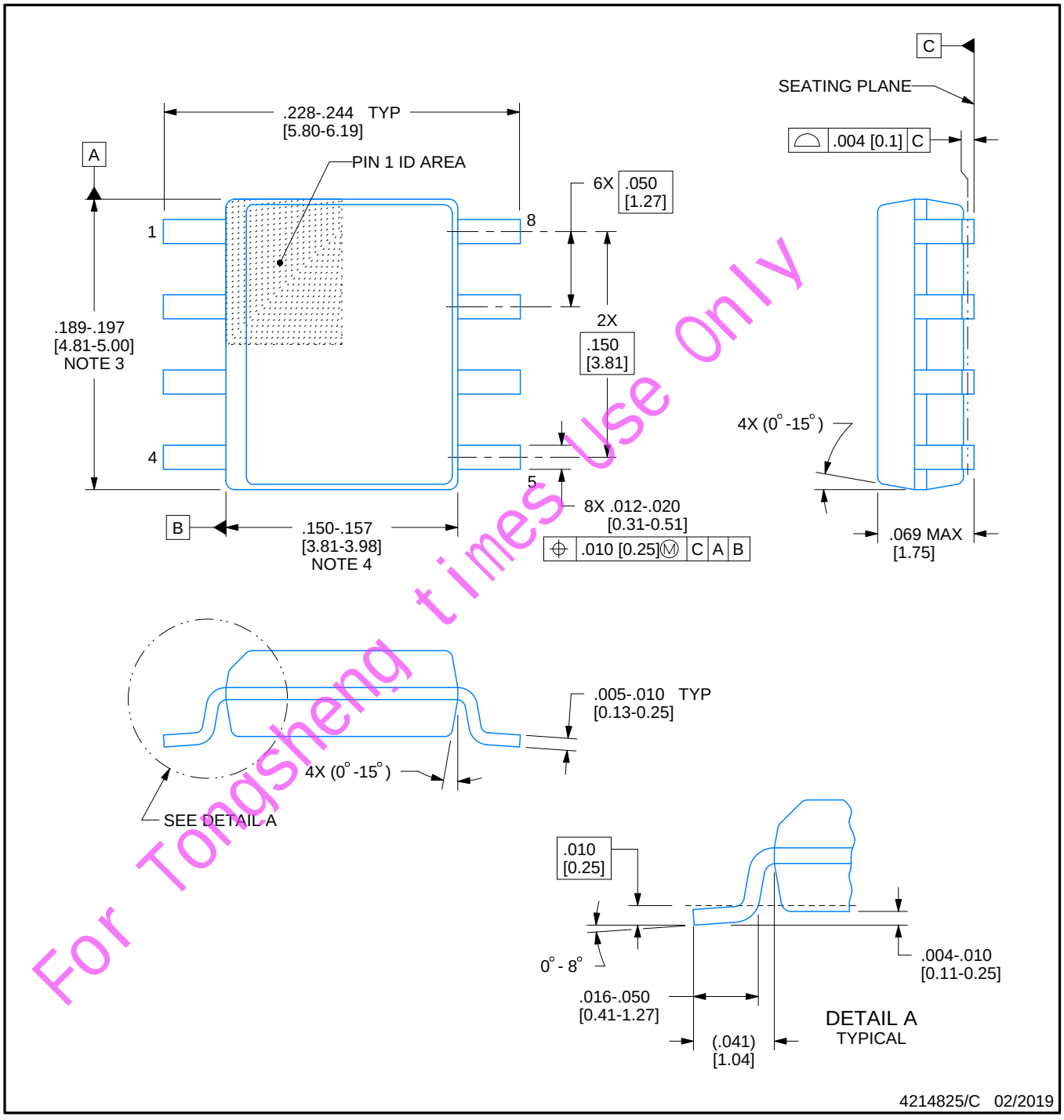


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

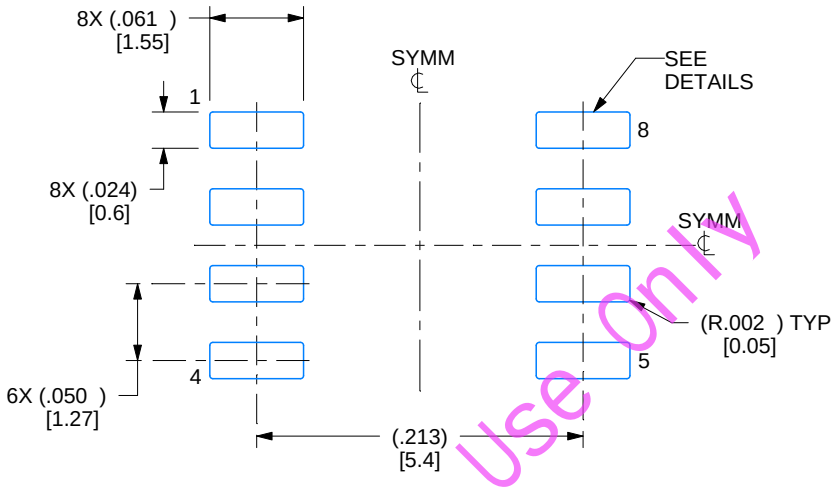
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

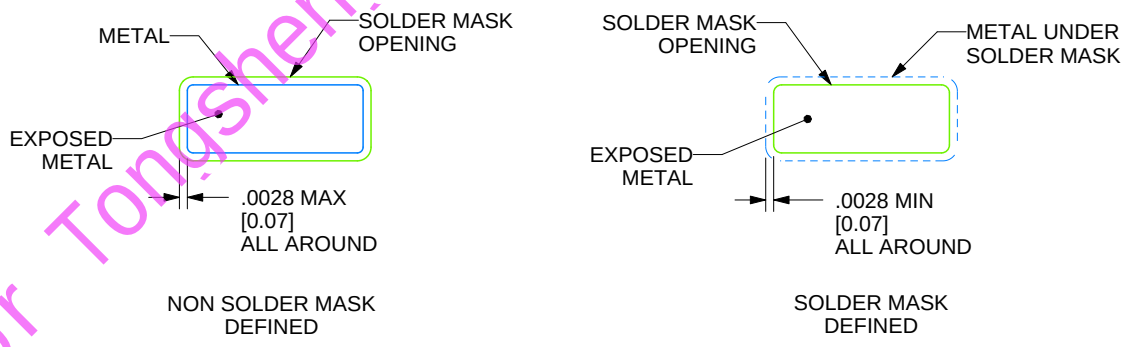
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

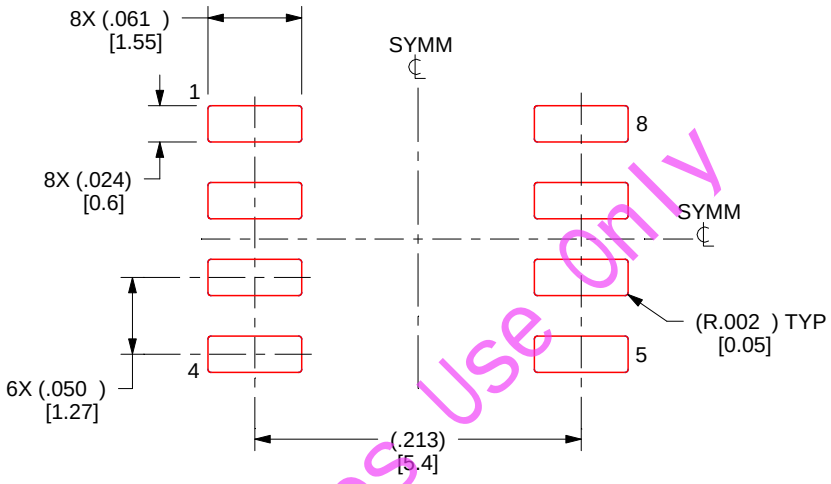
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



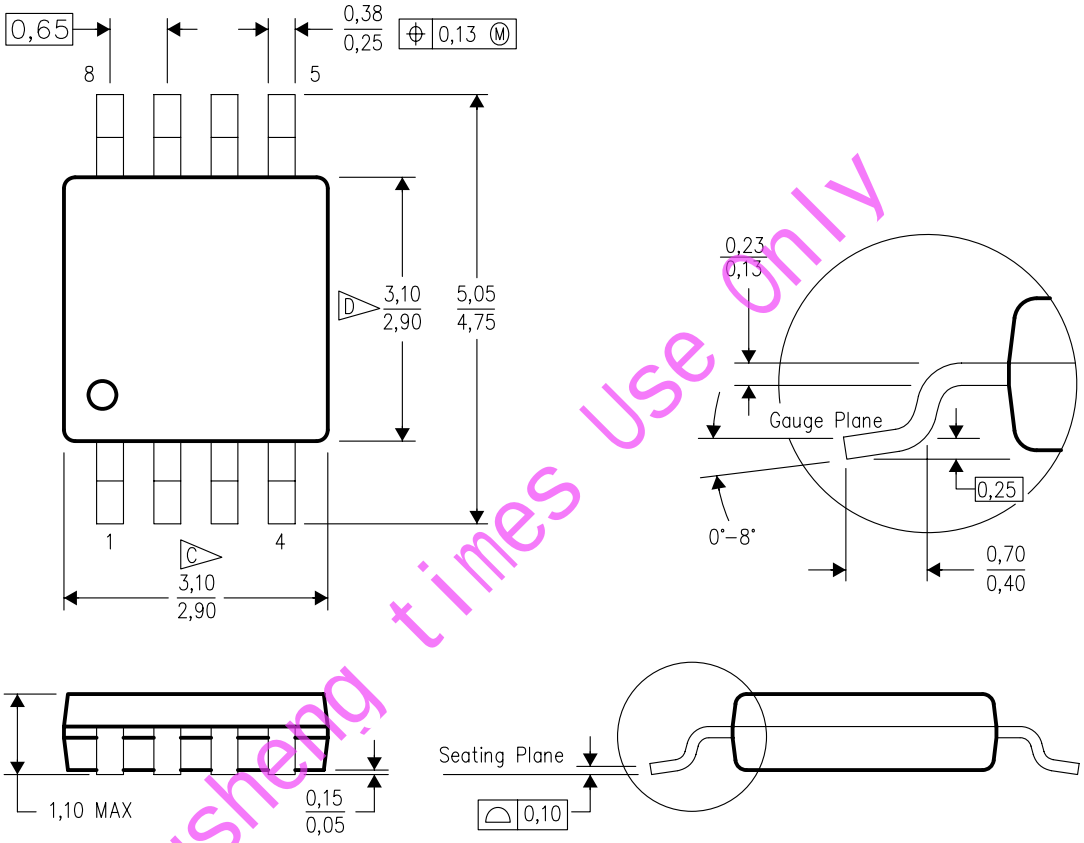
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

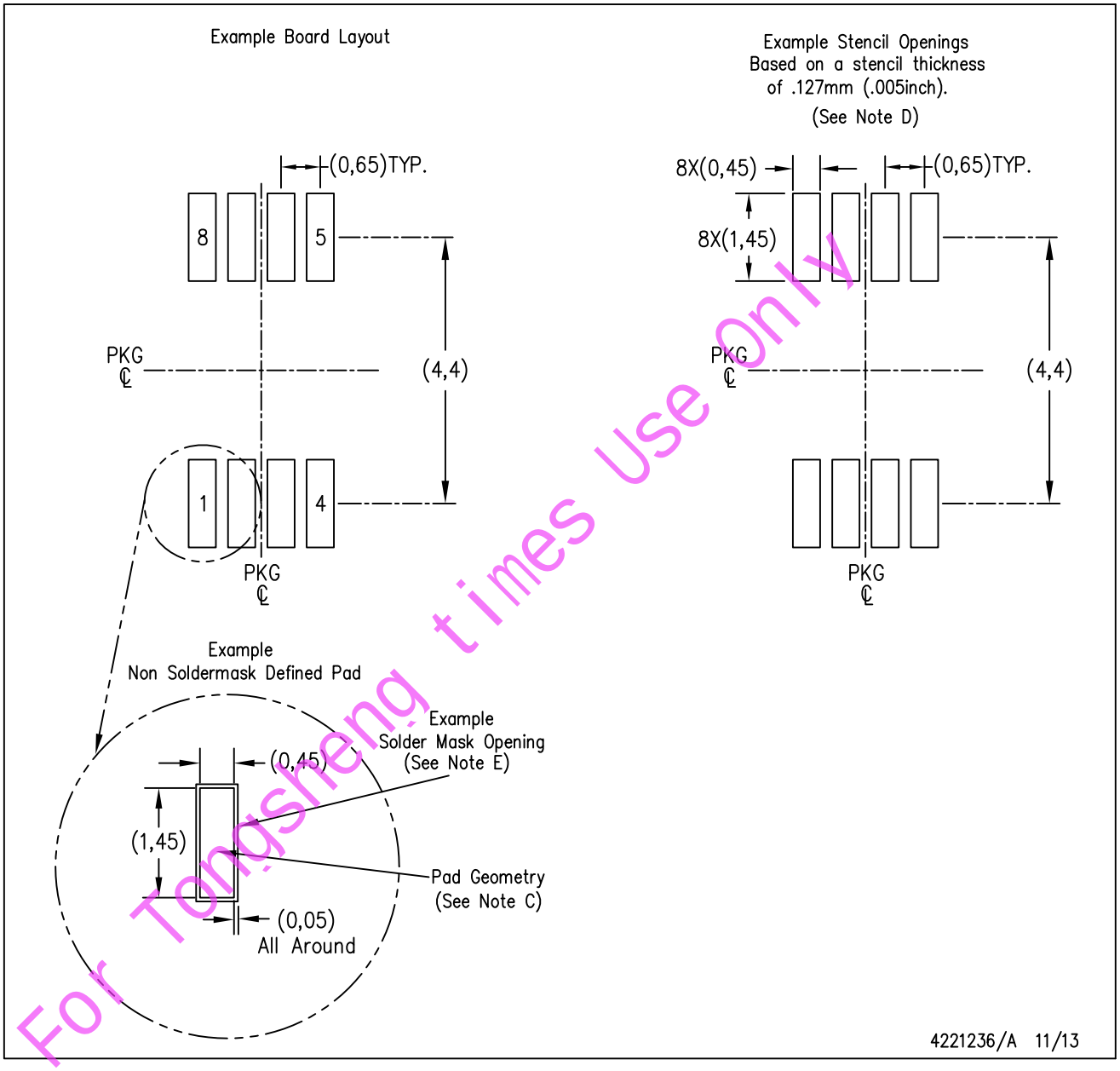
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.