

200V N-Channel Enhancement Mode MOSFET

Description

The AP100N20MP uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 10V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 200V$ $I_D = 100A$

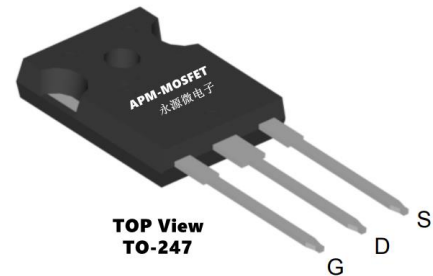
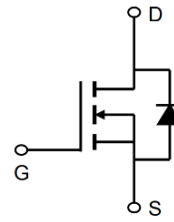
$R_{DS(ON)} < 20m\Omega$ @ $V_{GS}=10V$ (Type: 17m Ω)

Application

Load Switch

PWM Application

Power management



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP100N20MP	TO-247-3L	AP100N20MP XXX YYYY	360

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	200	V
$I_D@T_A=25^\circ C$	Continuous Drain Current $V_{GS} @ 10V$	100	A
$I_D@T_A=70^\circ C$	Continuous Drain Current $V_{GS} @ 10V$	52	A
I_{DM}^{*1}	Pulsed Drain Current (pulse width limited by T_{JM})	300	A
V_{GS}	Gate-to-Source Voltage	± 30	V
EAS	Single Pulse Avalanche Energy	300	mJ
EAr1	Avalanche Energy, Repetitive	75	mJ
IAR a1	Avalanche Current	45	A
dv/dt^{a2}	Peak Diode Recovery dv/dt	5.0	V/ns
PD	Power Dissipation	375	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	175, -55 To +175	$^\circ C$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.45	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	60	$^\circ C/W$



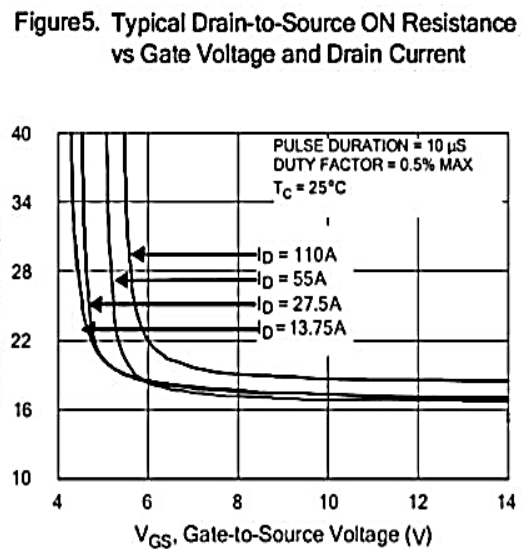
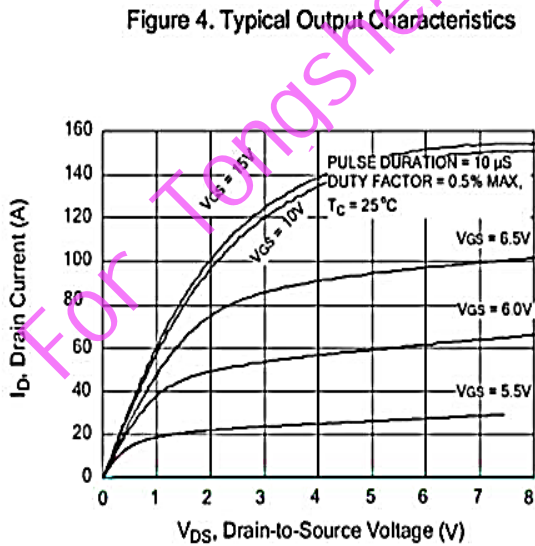
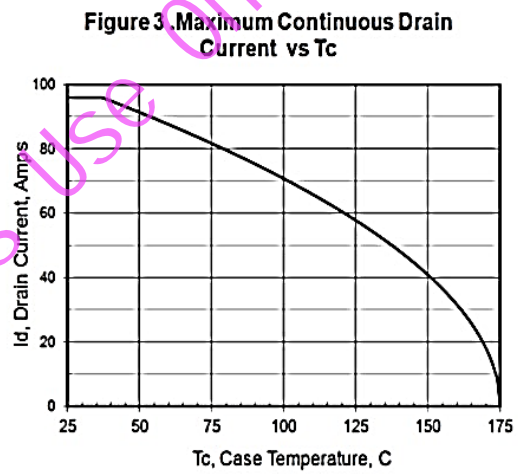
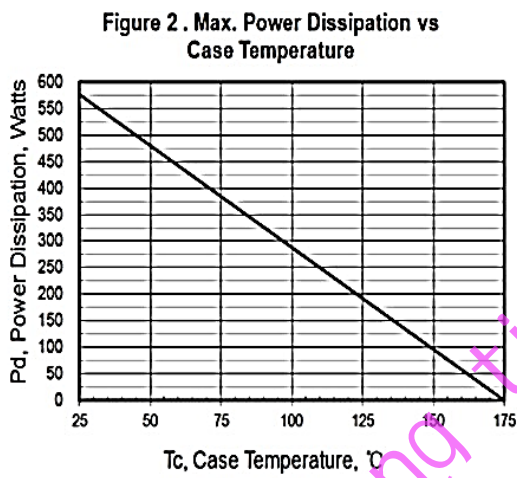
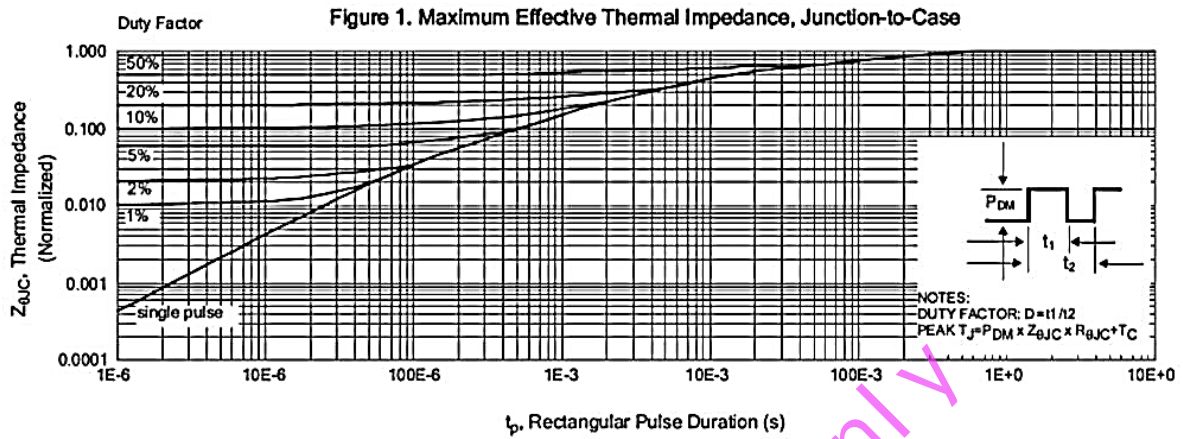
200V N-Channel Enhancement Mode MOSFET**Electrical Characteristics@T_j=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
VDSS	Drain to Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	200	220	--	V
IDSS	Drain to Source Leakage Current	V _{DS} =200V, V _{GS} =0V, T _a =25°C	--	--	1.0	μA
		V _{DS} =200V, V _{GS} =0V, T _a =125°C	--	--	100	μA
IGSS(F)	Gate to Source Forward Leakage	V _{GS} =+20V	--	--	100	nA
IGSS(R)	Gate to Source Reverse Leakage	V _{GS} =-20V	--	--	-100	nA
RDS(ON)	Drain-to-Source On-Resistance	V _{GS} =10V, I _D =40A	--	17	20	mΩ
VGS(TH)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	3.6	4.5	5.0	V
gfs	Forward Trans conductance	V _{DS} =25V, I _D =40A	50	65	--	S
R _g	Gate Resistance	V _{GS} =0V V _{DS} open f=1.0MHz	--	1.3	--	Ω
Ciss	Input Capacitance	V _{GS} =0V V _{DS} =25V f=1.0MHz	--	7500	--	pF
Coss	Output Capacitance		--	500	--	pF
Crss	Reverse Transfer Capacitance		--	210	--	pF
td(ON)	Turn-on Delay Time		--	45	--	ns
t _r	Rise Time	I _D =40A, V _{DS} =50V V _{GS} =10V, R _g =2.5Ω	--	70	--	ns
td(OFF)	Turn-Off Delay Time		--	110	--	ns
t _f	Fall Time		--	90	--	ns
Q _g	Total Gate Charge	I _D =40A, V _{DD} =100V V _{GS} =10V	--	85	--	nC
Q _{gs}	Gate to Source Charge		--	15	--	nC
Q _{gd}	Gate to Drain ("Miller") Charge		--	25	--	nC
ISD	Continuous Source Current (Body Diode)		--	--	75	A
ISM	Maximum Pulsed Current (Body Diode)		--	--	300	A
VSD	Diode Forward Voltage	I _S =40A, V _{GS} =0V	--	--	1.2	V
t _{rr}	Reverse Recovery Time	I _S =30A, T _J =25°C, V _{DD} =50V di _F /dt=100A/μs, V _{GS} =0V	--	110	--	ns
Q _{rr}	Reverse Recovery Charge		--	0.55	--	uC

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、The EAS data shows Max. rating . The test condition is T_J = 25°C, L=0.3mH, R_G=25Ω, V_{DD}=50V, V_{GS}=10V
- 4、The ISD=40A, di/dt≤100A/us, V_{DD}≤BV_{DS}, Start T_J=25°C
- 5、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Characteristics Curve:



200V N-Channel Enhancement Mode MOSFET Figure 6. Peak Current Capability

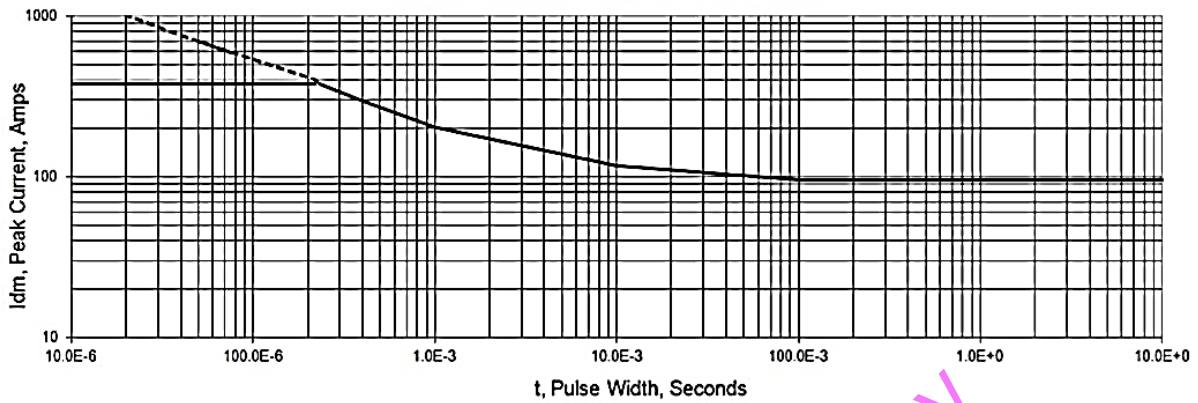


Figure 7. Typical Transfer Characteristics

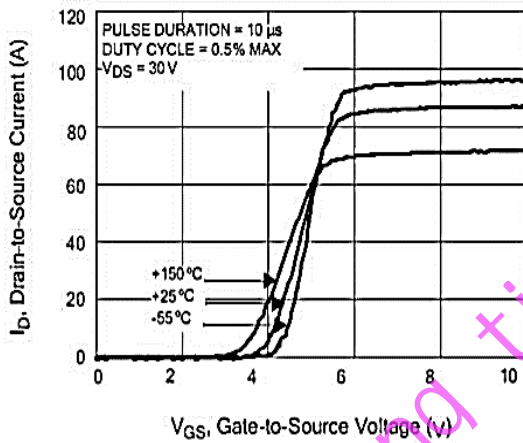


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

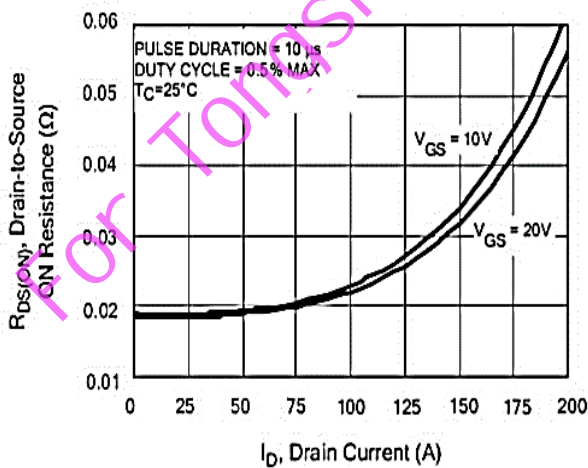


Figure 8. Unclamped Inductive Switching Capability

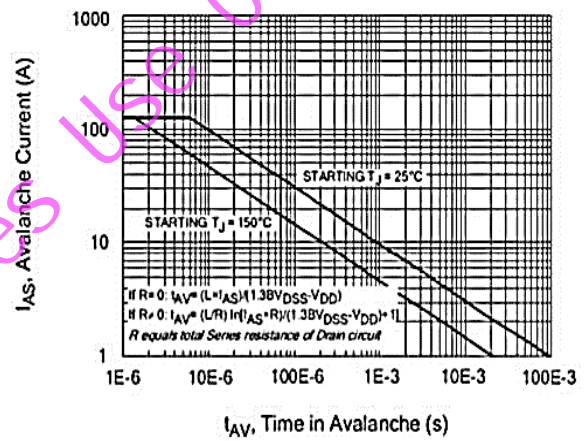
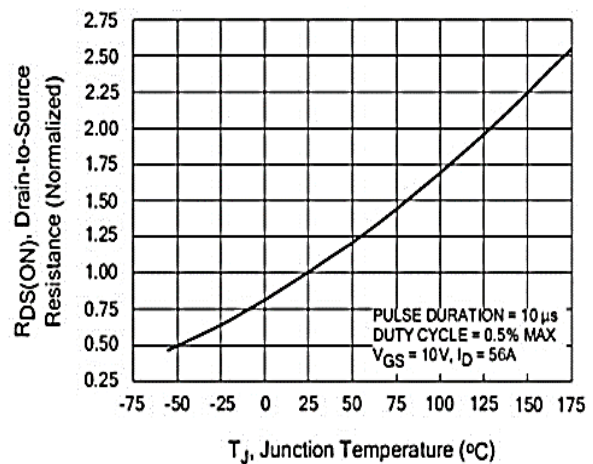


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature



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Figure 11. Typical Breakdown Voltage vs Junction Temperature

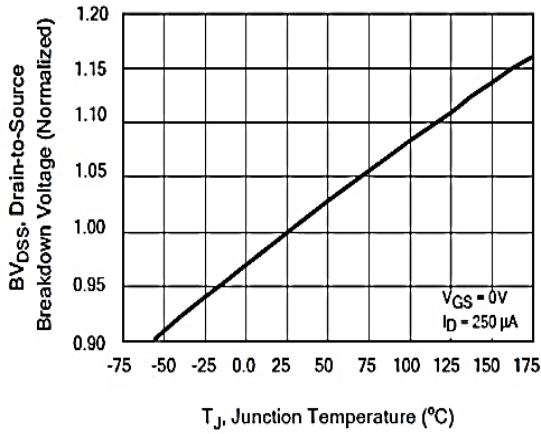


Figure 12. Typical Threshold Voltage vs Junction Temperature

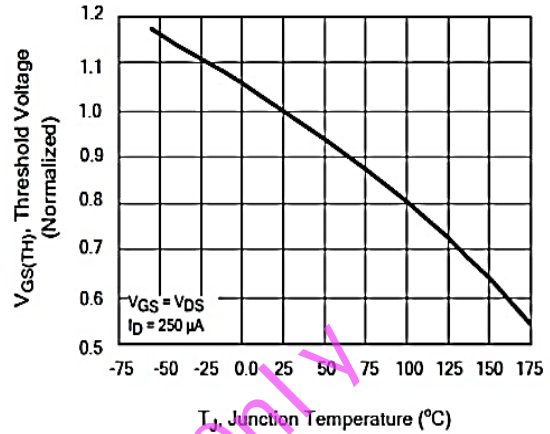


Figure 13. Maximum Safe Operating Area

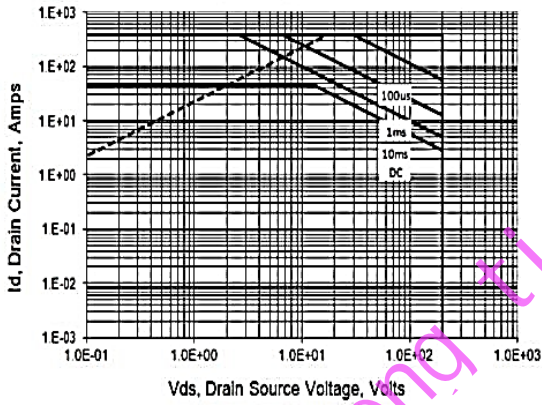


Figure 14. Capacitance vs Vds

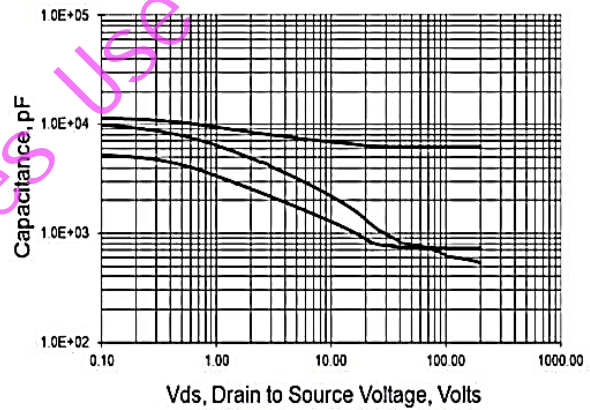


Figure 15. Typical Gate Charge

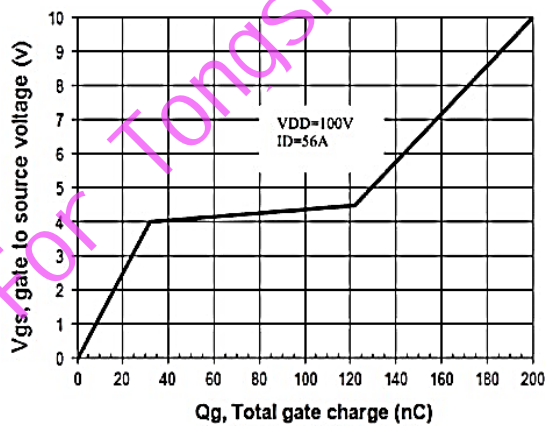
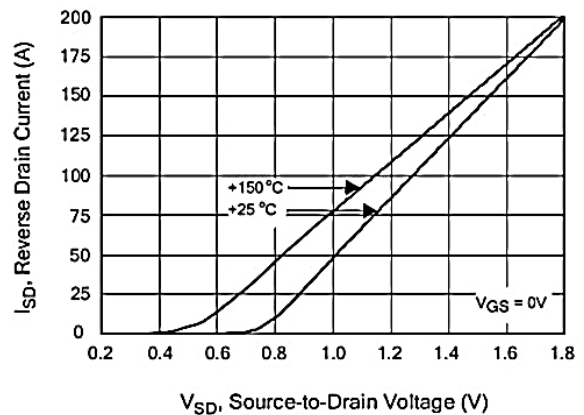
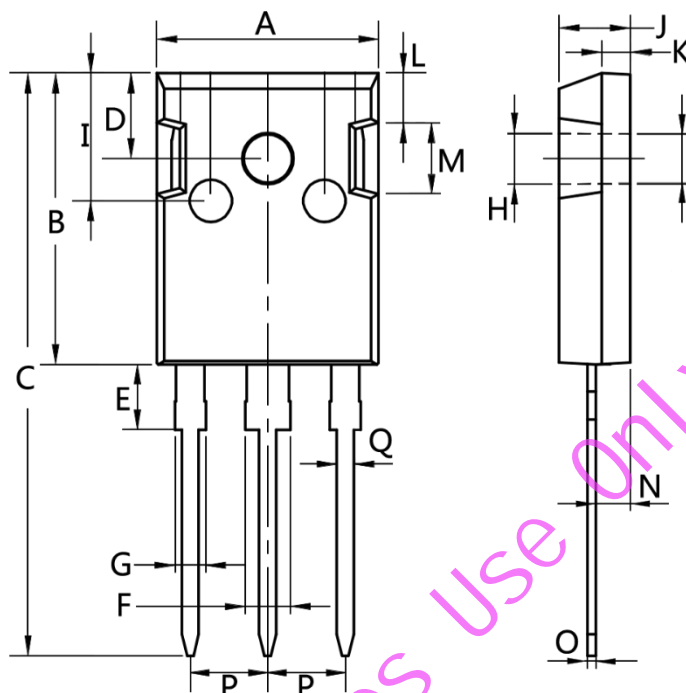


Figure 16. Typical Body Diode Transfer Characteristics



Package Mechanical Data-TO-247-3L



Dim.	Min.	Max.
A	15.0	16.0
B	20.0	21.0
C	41.0	42.0
D	5.0	6.0
E	4.0	5.0
F	2.5	3.5
G	1.75	2.5
H	3.0	3.5
I	8.0	10.0
J	4.9	5.1
K	1.9	2.1
L	3.5	4.0
M	4.75	5.25
N	2.0	3.0
O	0.55	0.75
P	Typ 5.08	
Q	1.2	1.3

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Edition	Date	Change
Rve1.0	2020/10/31	Initial release

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