

NCE P-Channel Super Trench Power MOSFET

Description

The NCEP40P60Q uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification

Application

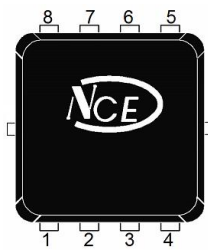
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

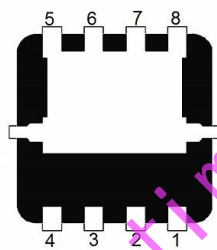
- $V_{DS} = -40V, I_D = -60A$
- $R_{DS(on)} = 8.8m\Omega$ (typical) @ $V_{GS} = -10V$
- $R_{DS(on)} = 12.5m\Omega$ (typical) @ $V_{GS} = -4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔVs TESTED!

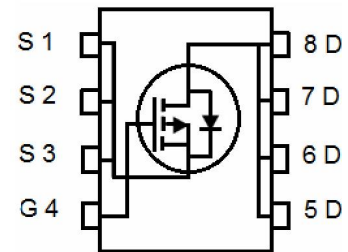
DFN 3.3X3.3-8L



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP40P60Q	NCEP40P60Q	DFN3.3X3.3-8L	-	-	-

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	$I_D(T_c=25^\circ C)$	-60	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D(T_c=100^\circ C)$	-42	A
Pulsed Drain Current	I_{DM}	-240	A
Maximum Power Dissipation($T_c=25^\circ C$)	$P_D(T_c=25^\circ C)$	75	W
Derating factor		0.6	W/ $^\circ C$
Single pulse avalanche energy ^(Note 1)	E_{AS}	352	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.67	$^\circ C/W$
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Electrical Characteristics (T_c=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-40		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0	-1.7	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-20A	-	8.8	11.0	mΩ
		V _{GS} =-4.5V, I _D =-20A	-	12.5	17.0	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-20A		30	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =-20V, V _{GS} =0V, F=1.0MHz	-	2450	-	PF
Output Capacitance	C _{oss}		-	660	-	PF
Reverse Transfer Capacitance	C _{rss}		-	18	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-20V, I _D =-20A V _{GS} =-10V, R _G =1.6Ω	-	9	-	nS
Turn-on Rise Time	t _r		-	4	-	nS
Turn-Off Delay Time	t _{d(off)}		-	30	-	nS
Turn-Off Fall Time	t _f		-	5	-	nS
Total Gate Charge	Q _g	V _{DS} =-20V, I _D =-20A, V _{GS} =-10V	-	39	-	nC
Gate-Source Charge	Q _{gs}		-	7.8		nC
Gate-Drain Charge	Q _{gd}		-	5.3		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =-20A	-		-1.2	V
Diode Forward Current	I _S		-	-	-60	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = -20A	-	22		nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs	-	58		nC

Notes:

1. EAS condition : T_J=25°C, V_{DD}=-20V, V_G=-10V, L=0.5mH, R_G=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_J(MAX)=150°C. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

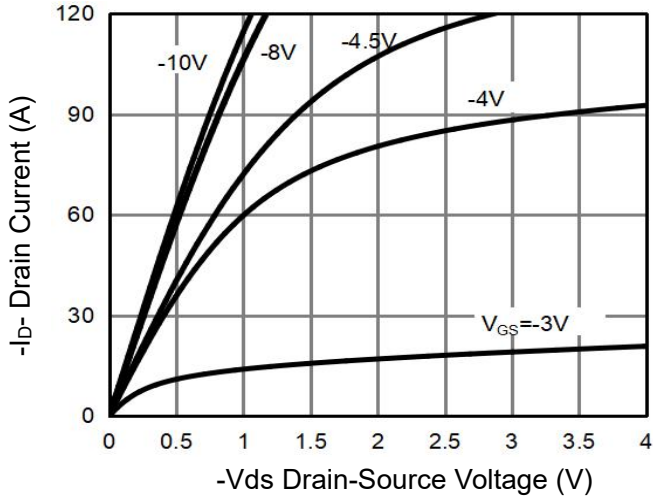


Figure 1 Output Characteristics

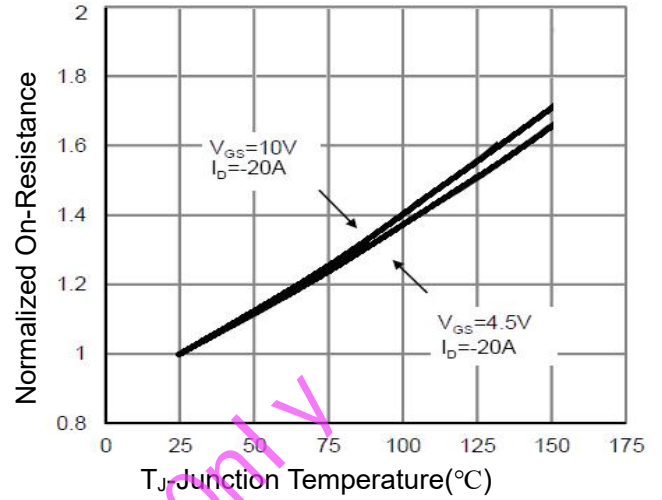


Figure 4 $R_{DS(on)}$ -Junction Temperature

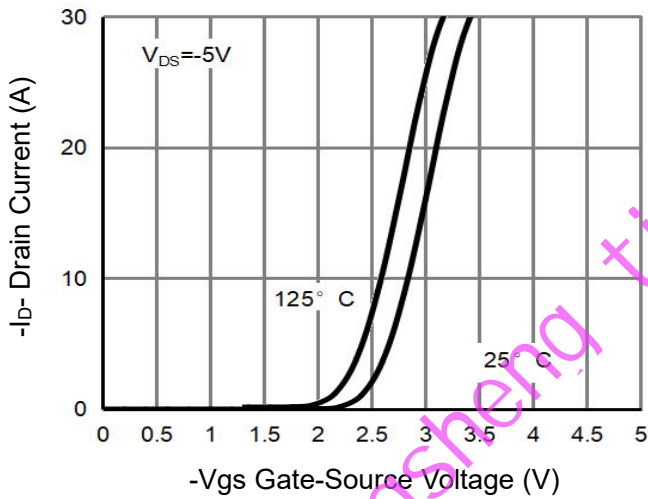


Figure 2 Transfer Characteristics

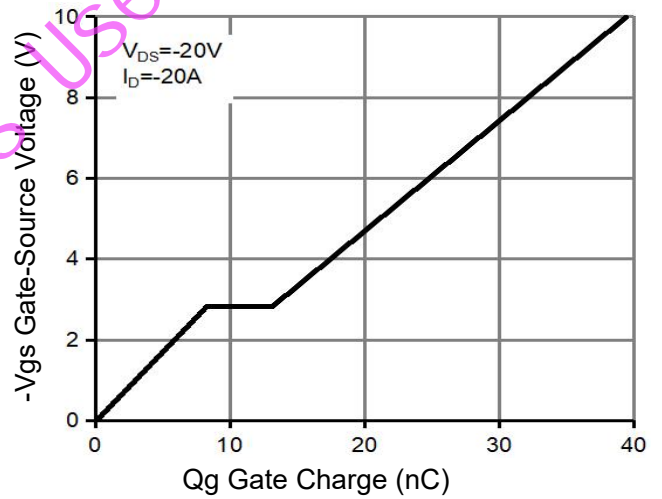


Figure 5 Gate Charge

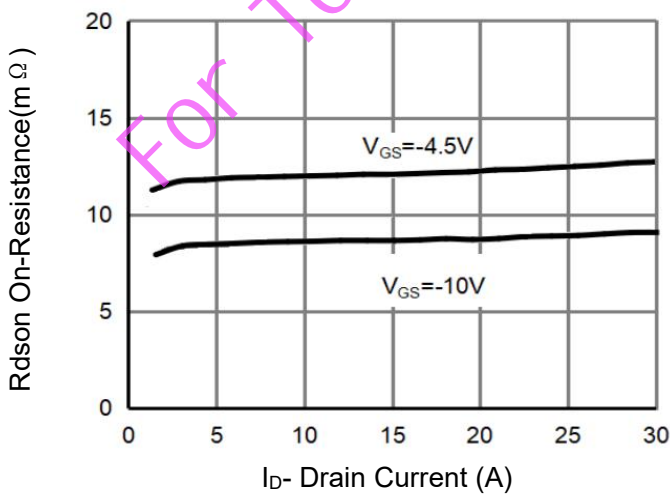


Figure 3 $R_{DS(on)}$ - Drain Current

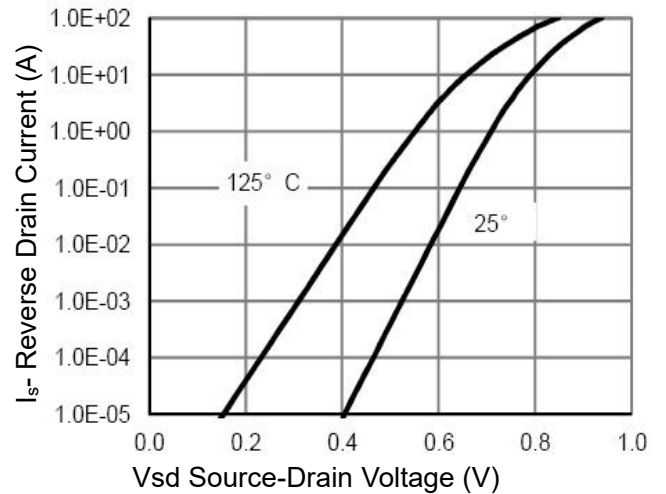


Figure 6 Source- Drain Diode Forward

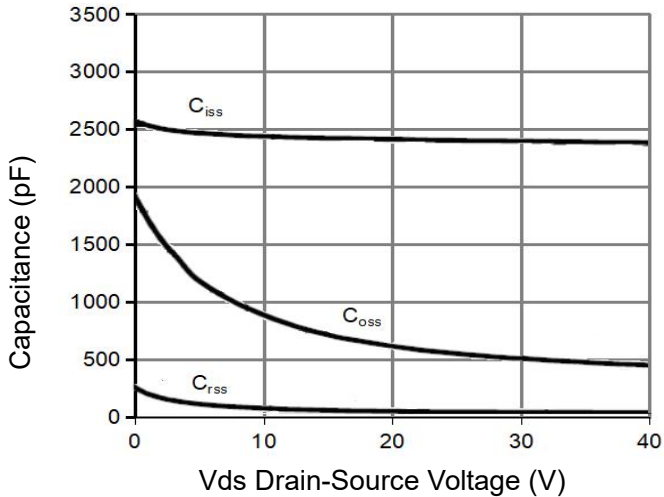


Figure 7 Capacitance vs Vds

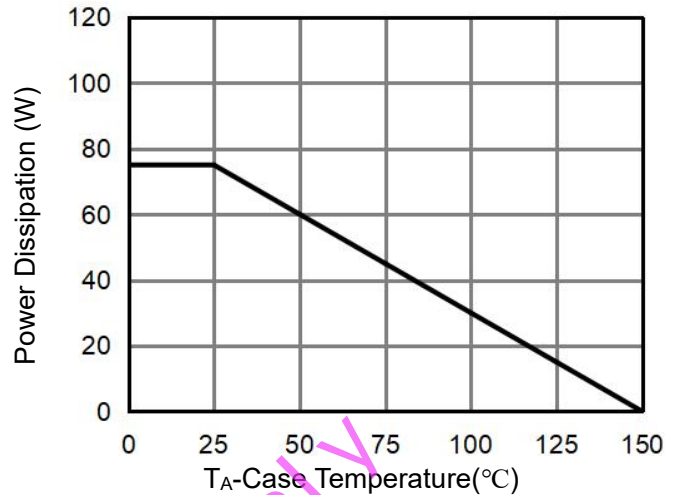


Figure 9 Power De-rating

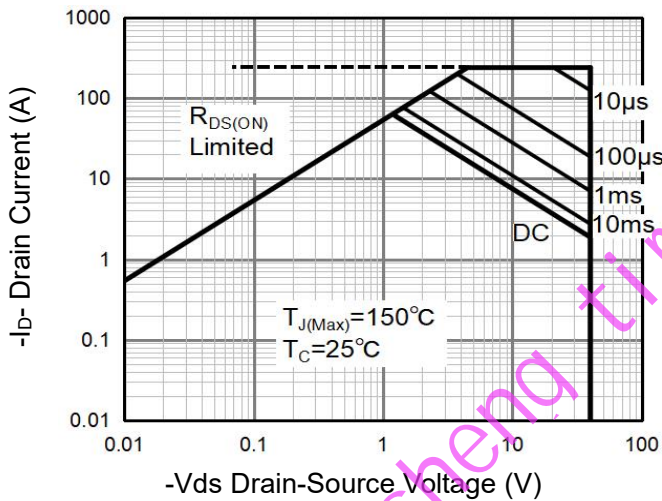


Figure 8 Safe Operation Area (Note 3)

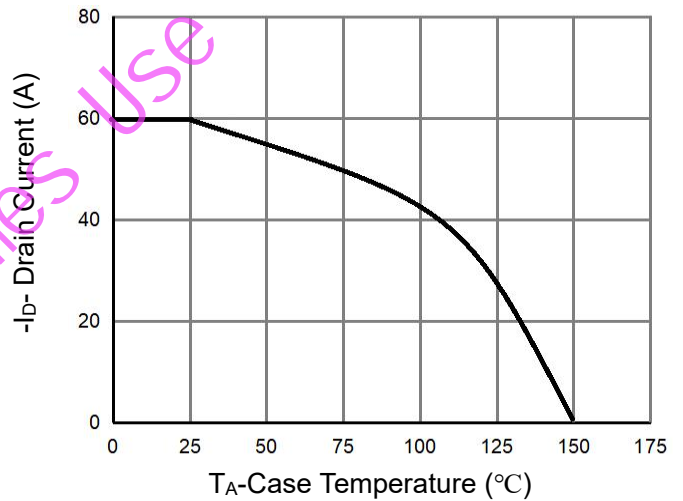


Figure 10 Current De-rating

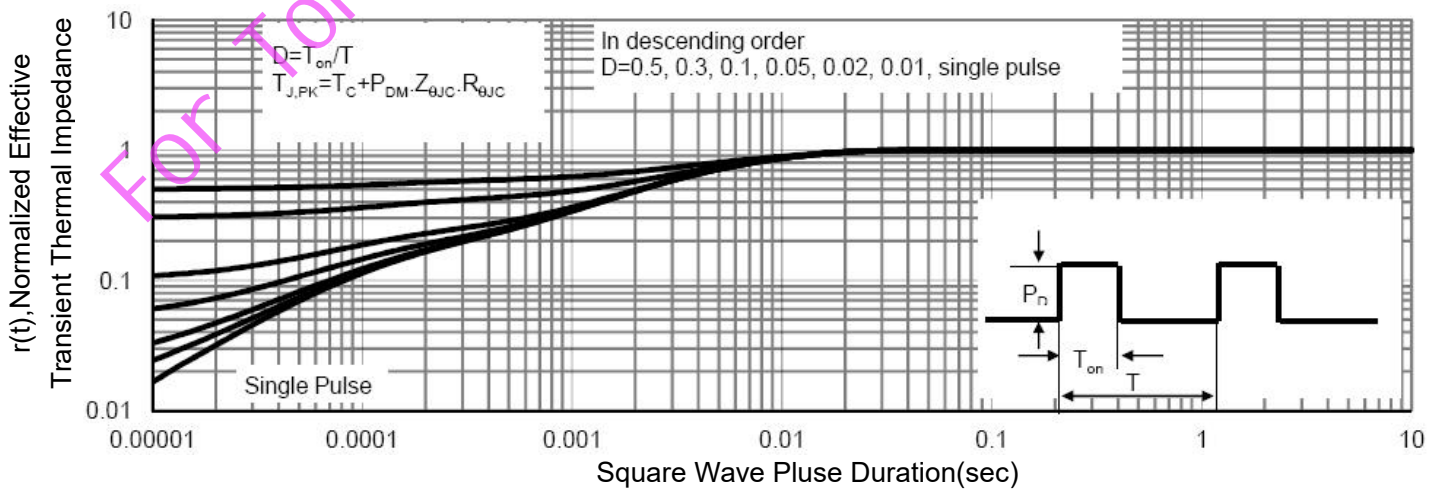
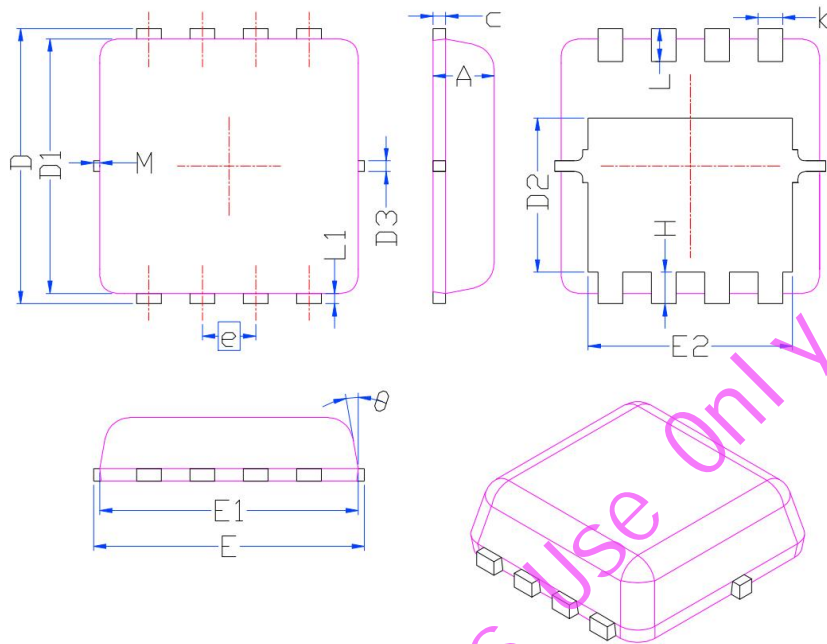


Figure 11 Normalized Maximum Transient Thermal Impedance

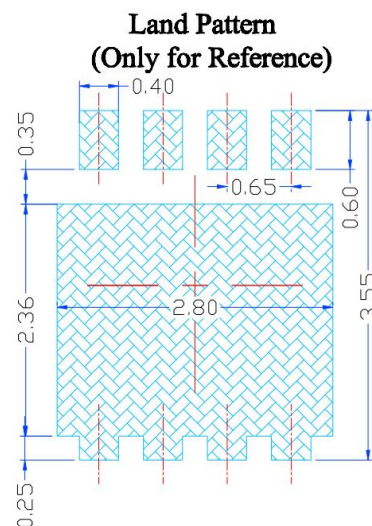
DFN3.3X3.3-8L Package Information



Note:

1. All Dimension Are In mm.
2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs.
Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Tie Bar Burrs, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.

SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.10	3.20	3.30
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			



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